COM Express™ Carrier Design Guide

Guidelines for designing COM Express™ Carrier Boards

March 13, 2009

Rev. 1.0

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Contents

1. Preface

1.1. About This Document

This document provides information for designing a custom system Carrier Board for COM Express Modules. It includes reference schematics for the external circuitry required to implement the various COM Express peripheral functions. It also explains how to extend the supported buses and how to add additional peripherals and expansion slots to a COM Express based system.

It's strongly recommended to use the latest COM Express specification and the Module vendors' product manuals as a reference.

This design guide is not a specification. It contains additional detail information but does not replace the PICMG COM Express (COM.0) specification.

For complete guidelines on the design of COM Express compliant Carrier Boards and systems, refer also to the full specification – do not use this design guide as the only reference for any design decisions.

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1.9. Acronyms and Abbreviations Used

Table 1: Acronyms and Abbreviations Used

Term	Description
AC '97 / HDA	Audio CODEC '97/High Definition Audio
CRT	Cathode Ray Tube
DAC	Digital Analog Converter
DDC	Display Data Channel is an I2C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
EFT	Electrical Fast Transient
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
GBE	Gigabit Ethernet
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LVDS	Low-Voltage Differential Signaling
N.A.	Not available
N.C.	Not connected
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
SATA	Serial AT Attachment: serial-interface standard for hard disks
SDVO	Serial Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system.
SMBus	System Management Bus
T.B.D.	To be determined
USB	Universal Serial Bus
x1, x2, x4, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x16 link.

1.10. Signal Table Terminology

Table 2 below describes the terminology used in this section for the Signal Description tables. The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

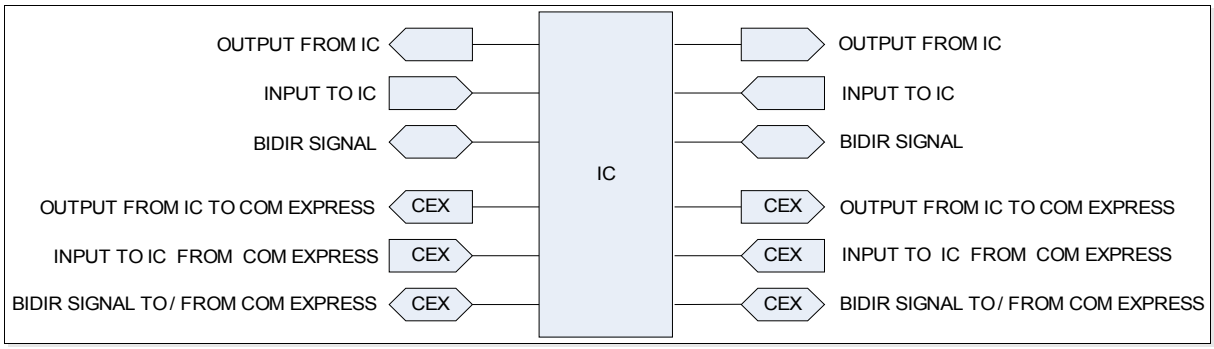
Table 2: Signal Table Terminology Descriptions

Term	Description
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3V3_SBY	Bi-directional 3.3V tolerant active during Suspend and running state.
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power input/output
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
USB	In compliance with the Universal Serial Bus Specification, Revision 2.0
GBE	In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet
SATA	In compliance with Serial ATA specification, Revision 1.0a
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities (pin-out type) to the Carrier Board.

Schematic Conventions

Schematic examples are drawn with signal directions shown per the figure below. Signals that connect directly to the COM Express connector are flagged with the text “CEX” in the off-page connect symbol, as shown in Figure 1 below. Nets that connect to the COM Express Module are named per the PICMG COM Express specification.

Figure 1: Schematic Conventions



Power nets are labeled per the table below. The power rail behavior under the various system power states is shown in the table.

Table 3: Naming of Power Nets

Power Net	S0 On	S3 Suspend to RAM	S4 Suspend to Disk	S5 Soft Off	G3 Mechanical Off
VCC_12V	12V	off	off	off	off
VCC_5V0	5V	off	off	off	off
VCC_3V3	3.3V	off	off	off	off
VCC_1V5	1.5V	off	off	off	off
VCC_2V5	2.5V	off	off	off	off
VCC_5V_SBY	5V	5V	5V	5V	off
VCC_3V3_SBY	3.3V	3.3V	3.3V	3.3V	off
VCC_RTC	3.0V	3.0V	3.0V	3.0V	3.0V

2. COM Express Interfaces

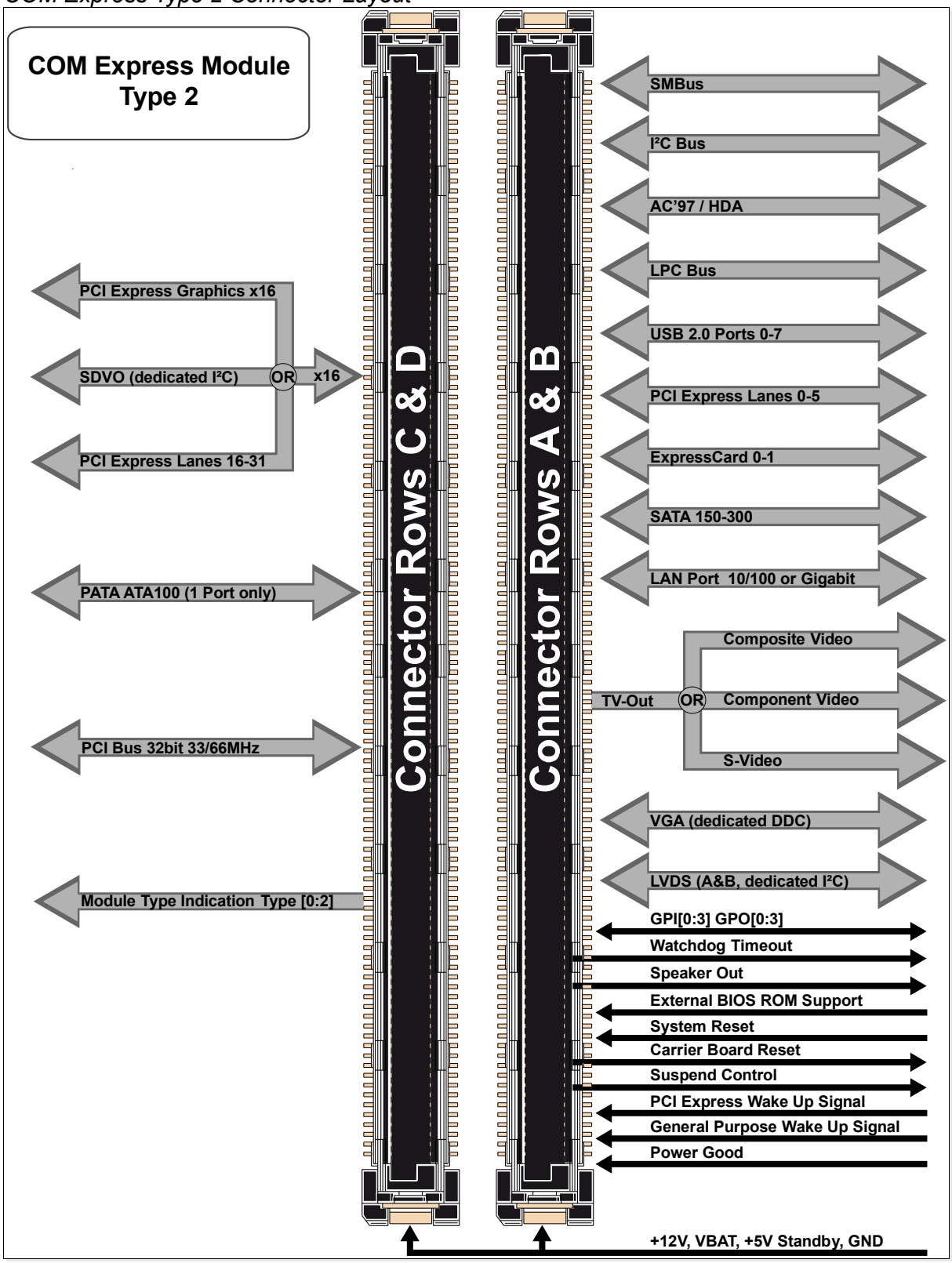
The following section describes the signals found on COM Express Type 2 connectors. Most of the signals listed in the following sections also apply to other COM Express Module types. The pin-out for connector rows A and B remains the same regardless of the Module type but the pin-out for connector rows D and C are dependent on the Module type. Refer to the COM Express Specification for information about the different pinouts of the Module types other than Type 2.

2.1. COM Express Signals

The source document for the definition of the COM Express signals is the ***PICMG COM.0 R1.0 COM Express Module Base Specification***.

Figure 2 below summarizes the Type 2 signals and shows a graphical representation of the A-B and C-D COM Express connectors. Each of the signal groups in the figure is described and usage examples are given in the sub-sections of this section.

Figure 2: COM Express Type 2 Connector Layout



2.2. PCIe General Introduction

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. A PCI Express lane consists of dual simplex channels, each implemented as a low-voltage differentially driven transmit pair and receive pair. They are used for simultaneous transmission in each direction. The bandwidth of a PCI Express link can be scaled by adding signal pairs to form multiple lanes between two devices. The PCI Express specification defines x1, x4, x8, x16, and x32 link widths. Each single lane has a raw data transfer rate of 2.5Gbps @ 1.25GHz.

PCIe is easy to work with, but design rules must be followed. The most important design rule is that the PCIe lanes must be routed as differential pairs. PCIe design rules are covered in detail in Section 2.3.6 'PCI Express Routing Considerations' at page 32. Routing a PCIe link is often easier than routing a traditional 32 bit wide PCI bus, as there are fewer lines (2 data pairs and a clock pair for a PCIe x1 link as opposed to over 50 lines for parallel PCI). Routing a PCIe x16 graphics link is much easier than routing an AGP 8X link, as the constraints required for the PCIe implementation are much easier than those for AGP.

The source specifications for PCI Express include the ***PCI Express Base Specification,*** the ***PCI Express Card Electromechanical Specification*** and the ***PCI Express Mini Card Electromechanical Specification.***

2.2.1. COM Express A-B Connector and C-D Connector PCIe Groups

COM Express Type 2 Modules have two groups of PCIe lanes. There is a group of up to six lanes on the COM Express A-B connector that are intended for general purpose use, such as interfacing the COM Express Module to Carrier Board PCIe peripherals. A second group of PCIe lanes is defined on the COM Express C-D connector. This group is intended primarily for the PCIe Graphics interface (also referred to as the PEG interface), and is typically 16 PCIe lanes wide. For some Modules, the PEG lanes may be used for general purpose PCIe lanes if the external graphics interface is not in use. This usage is Module and Module chipset dependent.

2.3. General Purpose PCIe Lanes

2.3.1. General Purpose PCIe Signal Definitions

The general purpose PCI Express interface of the COM Express Type 2 Module on the COM Express A-B connector consists of up to 6 lanes, each with a receive and transmit differential signal pair designated from PCIE_RX0 (+ and -) to PCIE_RX5 (+ and -) and correspondingly from PCIE_TX0 (+ and -) to PCIE_TX5 (+ and -). The 6 lanes may be grouped into various link widths as defined in the COM Express spec and summarized in Sections 2.3.3 and 2.3.2 below. The signals used are summarized in Table 4 below.

Table 4: General Purpose PCI Express Signal Descriptions

Signal	Pin#	Description	I/O	Comment
PCIE_RX0+ PCIE_RX0-	B68 B69	PCIe channel 0. Receive Input differential pair.	I PCIE	
PCIE_TX0+ PCIE_TX0-	A68 A69	PCIe channel 0. Transmit Output differential pair.	O PCIE	
PCIE_RX1+ PCIE_RX1-	B64 B65	PCIe channel 1. Receive Input differential pair.	I PCIE	
PCIE_TX1+ PCIE_TX1-	A64 A65	PCIe channel 1. Transmit Output differential pair.	O PCIE	
PCIE_RX2+ PCIE_RX2-	B61 B62	PCIe channel 2. Receive Input differential pair.	I PCIE	
PCIE_TX2+ PCIE_TX2-	A61 A62	PCIe channel 2. Transmit Output differential pair.	O PCIE	
PCIE_RX3+ PCIE_RX3-	B58 B59	PCIe channel 3. Receive Input differential pair.	I PCIE	
PCIE_TX3+ PCIE_TX3-	A58 A59	PCIe channel 3. Transmit Output differential pair.	O PCIE	
PCIE_RX4+ PCIE_RX4-	B55 B56	PCIe channel 4. Receive Input differential pair.	I PCIE	
PCIE_TX4+ PCIE_TX4-	A55 A56	PCIe channel 4. Transmit Output differential pair.	O PCIE	
PCIE_RX5+ PCIE_RX5-	B52 B53	PCIe channel 5. Receive Input differential pair.	I PCIE	
PCIE_TX5+ PCIE_TX5-	A52 A53	PCIe channel 5. Transmit Output differential pair.	O PCIE	
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes.	O PCIE	COM Express only allocates a single ref clock
EXCD0_CPPE#	A49	PCI ExpressCard0: PCI Express capable card request, active low, one per card	I CMOS	
EXCD0_PERST#	A48	PCI ExpressCard0: reset, active low, one per card	O CMOS	
EXCD1_CPPE#	B48	PCI ExpressCard1: PCI Express capable card request, active low, one per card	I CMOS	
EXCD1_PERST#	B47	PCI ExpressCard1: reset, active low, one per card	O CMOS	
CB_RESET#	B50	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.	O CMOS	
PCI_RESET#	C23	PCI Reset output, active low.	O CMOS Suspend	
WAKE0#	B66	PCI Express wake up signal	I CMOS	

2.3.2. PCI Express Lane Configurations – Per COM Express Spec

According to the COM Express specification, the PCIe lanes on the A-B connector can be configured as up to six PCI Express x1 links or may be combined into various combinations of x4, x2 and x1 links that add up to a total of 6 lanes. These configuration possibilities are based on the COM Express Module's chip-set capabilities.

The COM Express specification defines a "fill order" from mapping PCIe links that are wider than x1 onto the COM Express pins. For example, the spec requires that a x4 PCI Express link be mapped to COM Express PCI Express lanes 0,1,2 and 3. Refer to the COM Express specification for details.

Note: All PCI Express devices are required to work in x1 mode as well as at their full capability. A x4 PCIe card for example is required by the PCI Express specification to be usable in x4 and / or x1 mode. The "in-between" modes (x2 in this case) are optional.

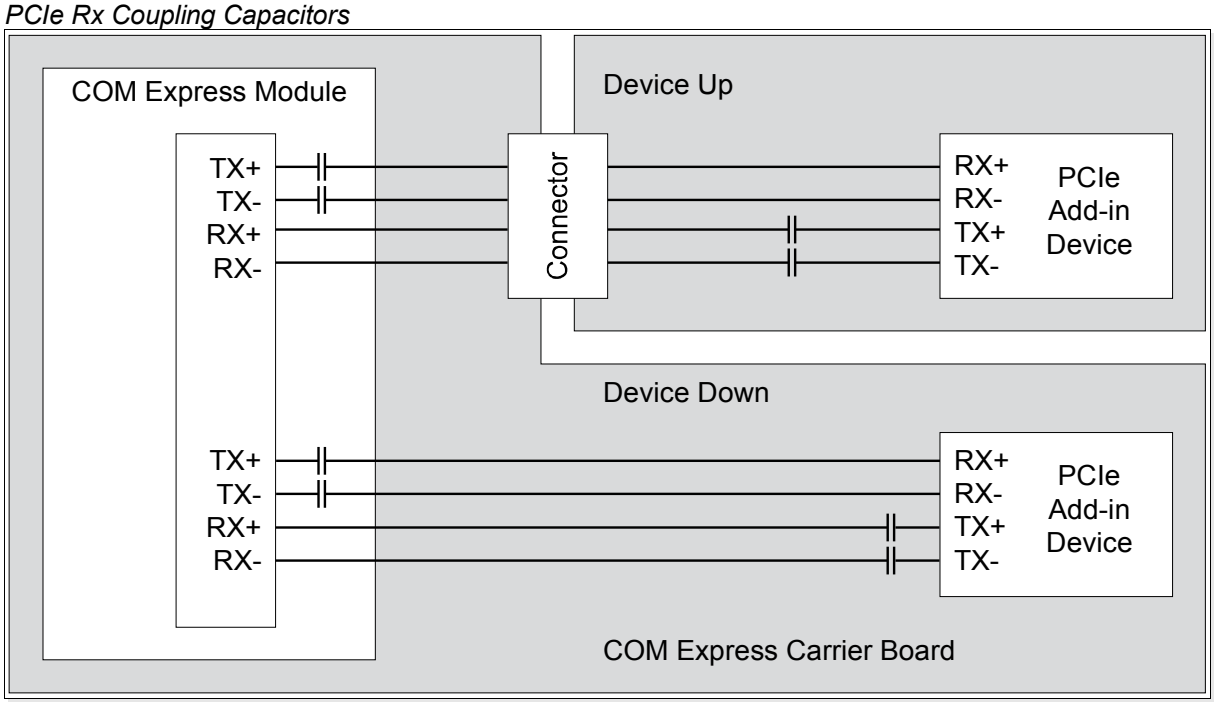
2.3.3. PCI Express Lane Configurations – Module and Chipset Dependencies

The lane configuration possibilities of the PCI Express interface of a COM Express Module are dependent on the Module's chip-set. Some Module and chip-set implementations may allow software or setup screen configuration of link width (x1, x4). Others may require a hardware strap or build option on the Module to configure the x4 option. The COM Express specification does not allocate any Module pins for strapping PCIe lane width options.

Refer to the vendor specific Module documentation for the Module that you are using for additional information about this subject.

2.3.4. Device Up / Device Down and PCIe Rx / Tx Coupling Capacitors

Figure 3: PCIe Rx Coupling Capacitors



"Device Down" refers to a PCIe target device implemented down on the Carrier Board. "Device Up" refers to a PCIe target device implemented on a slot card (or mini-PCIe card, ExpressCard, AMC card). There are several distinctions between a PCIe "Device Down" and "Device Up" implementation:

Device Down:

- Coupling caps for the target device PCIe TX lines (COM Ex Module PCIe RX lines) are down on the Carrier Board, close to the target device TX pins;
- Trace length allowed for PCIe signals on the Carrier Board is longer for the Device Down case than for Device Up. See Section 6.4.1. 'PCI Express 1.1 Trace Routing Guidelines' on page 132 for trace length details.

Device Up:

- Coupling caps for the target device PCIe TX lines (COM Ex Module PCIe RX lines) are up on the slot card.
- Trace length allowed for PCIe signals on the Carrier Board is shorter than for the Device Down case, to allow for slot card trace length. See Section 6.4.1 'PCI Express 1.1 Trace Routing Guidelines' on page 132 for trace length details.

The coupling caps for the Module PCIe TX lines are defined by the COM Express specification to be on the Module.

2.3.5. Schematic Examples

2.3.5.1. Reference Clock Buffer

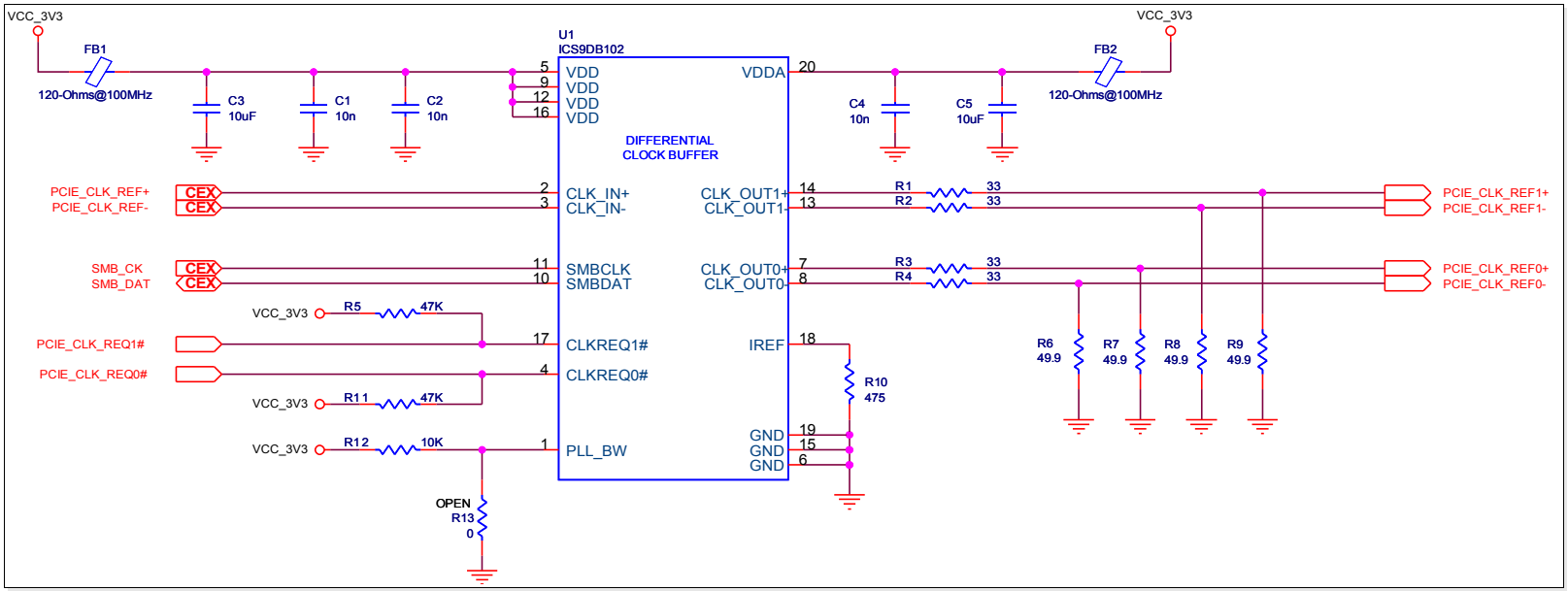
The COM Express Specification calls for one copy of the PCIe reference clock pair to be brought out of the Module. This clock is a 100MHz differential pair and is sometimes known as a “hint” clock. The clock allows the PLL in the target PCIe device to lock faster onto the embedded clock in the PCIe bit stream.

If the Carrier Board implements only one PCIe device or slot, then the PCIe reference clock pair from the Module may be routed directly to that device or slot. However, if there are two or more PCIe devices or slots on the Carrier Board, then the Module PCIe reference clock should be buffered using a PLL based “zero-delay” buffer. Such devices are available from IDT, Cypress Semiconductor, and others.

The IDT ICS9DB102, ICS9DB104 and ICS9DB106 have two, four and six differential output replicas of the input clock, respectively. The Cypress CY28401 provides eight copies of the differential input clock. Each target device (PCIe “device down” chip, slot, Express Card slot, PEG slot) should get an individual copy of the reference clock.

The reference clock pairs should be routed as directly as possible from source to destination.

Figure 4: PCIe Reference Clock Buffer



The following notes apply to Figure 4 'PCIe Reference Clock Buffer'.

Nets that tie directly to the COM Express connector are indicated with the CEX flag in the off-page connection symbol.

Each clock pair is routed point to point to each connector or end device using differential signal routing rules.

Each clock output pair in the example shown is terminated close to the ICS9DB102 buffer pins with a series resistor (shown as 33 Ω) and a termination to GND (shown as 49.9 Ω), per the vendor's recommendations. Other vendors may have different recommendations, particularly in regard to the source termination to GND.

SMBUS software can enable or disable clock-buffer outputs. Disable unused outputs to reduce emissions.

The CLKREQ0# and CLKREQ1# should be pulled low to enable the corresponding clock buffer outputs. For applications in which power management is not a concern, these inputs may be tied low to permanently enable the outputs.

2.3.5.2. Reset

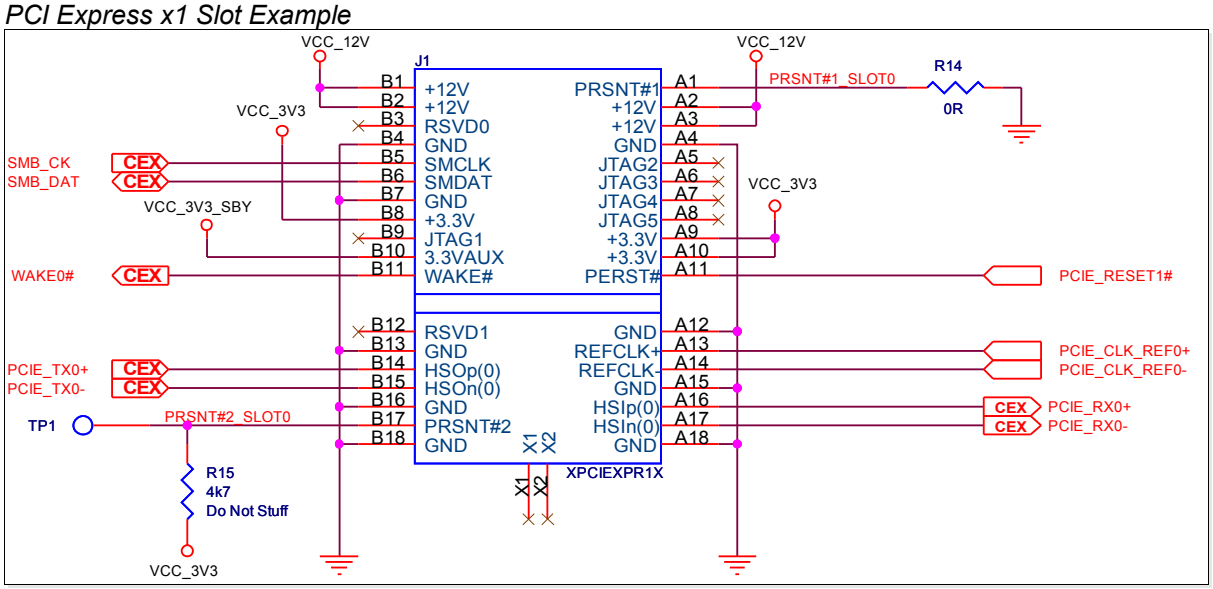
The PCI Interface of the COM Express Module shares the reset signal 'PCI_RESET#' with the PCI Express interface.

COM Express signal CB_RESET# may be used in place of PCI_RESET#. For Type 1, Type 4 and Type 5 COM Express pin-outs, CB_RESET# must be used, as PCI_RESET# is not available.

2.3.5.3. x1 Slot Example

An example of an x1 PCIe slot is shown in Figure 5 below. The source specification for slot implementations is the PCI-SIG ***PCI Express Card Electromechanical Specification.***

Figure 5: PCI Express x1 Slot Example



The example above shows COM Express PCIe lane 0 connected to the slot. Other lanes may be used, depending on what is available on the particular Module being used.

No coupling caps are required on the PCIe data or clock lines. The PCIe TX series coupling caps on the data lines are on the COM Express Module. The PCIe RX coupling caps are up on the slot card.

Slot signals REFCLK+ and REFCLK- (pins A13 and A14) are driven by the Clock Buffer, which is shown in Figure 4 'PCIe Reference Clock Buffer' on page 22. If there is only one PCIe target on the Carrier Board, the Clock Buffer may be omitted and the slot REFCLOCK signals may be driven directly by the COM Express Module.

The slot PWRGD signal (pin A11) is driven by a buffered copy of the COM Express PCI_RESET# signal. A buffered copy of CB_RESET# could also be used. If the Carrier board only has one or two target devices, an unbuffered PCI_RESET# or CB_RESET# could be used.

The slot signals PRSNT1# and PRSNT2# are part of a mechanism defined in the ***PCI Express Card Electromechanical Specification*** to allow hot-plugged PCIe cards. However, most systems do not implement the support circuits needed to complete hot-plug capability. If used, the scheme works as follows: in Figure 5 above, PRSNT1# (pin A1) is pulled low on the Carrier Board through R14. On the slot card, PRSNT1# is routed to PRSNT2#_0 (pin B17). The state of slot pin B17 may be read back by the BIOS or system software, if routed to an input port pin that can be read by software. If a slot card is present, this pin reads back low; if the slot is empty, the pin will be read high. Software then uses this information to apply power to the card. There is no standard input port pin defined by COM Express for this function. For systems that are not trying to implement hot-swap capability, it is not necessary to be able to read back the state of the PRSNT2# pin. Hence it is shown in the figure above as being brought to a test point.

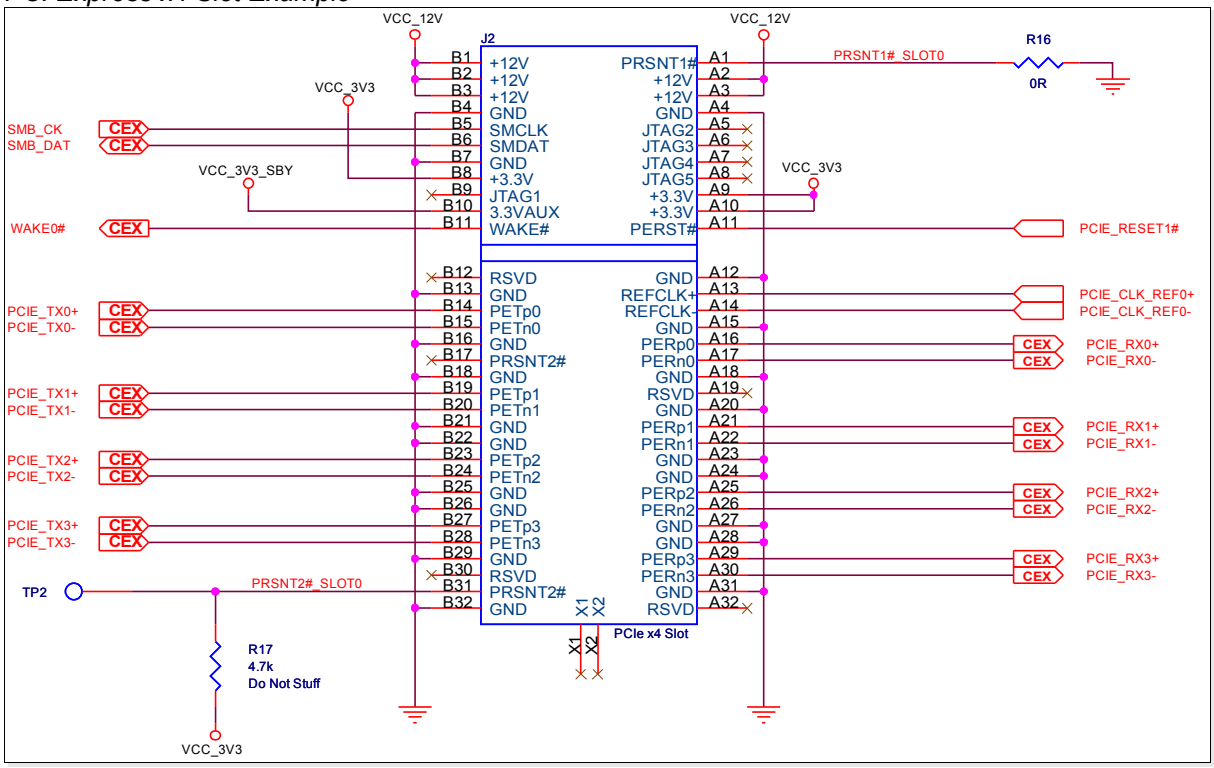
Nets SMB_CK and SMB_DAT are sourced from COM Express Module pins B13 and B14 respectively. The SMBUS supports card-management support functions. SMBUS software can save the state of the slot-card device before a Suspend event, report errors, accept control parameters, return status information and card information such as a serial number. Support for the SMBUS is optional on the slot card.

WAKE0# is asserted by the slot card to cause COM Express Module wake-up at Module pin B66. This is an open-drain signal. It is an input to the Module and is pulled up on the Module. Other WAKE0# sources may pull this line low; it is a shared line.

Slot JTAG pins on A5-A8 are not used.

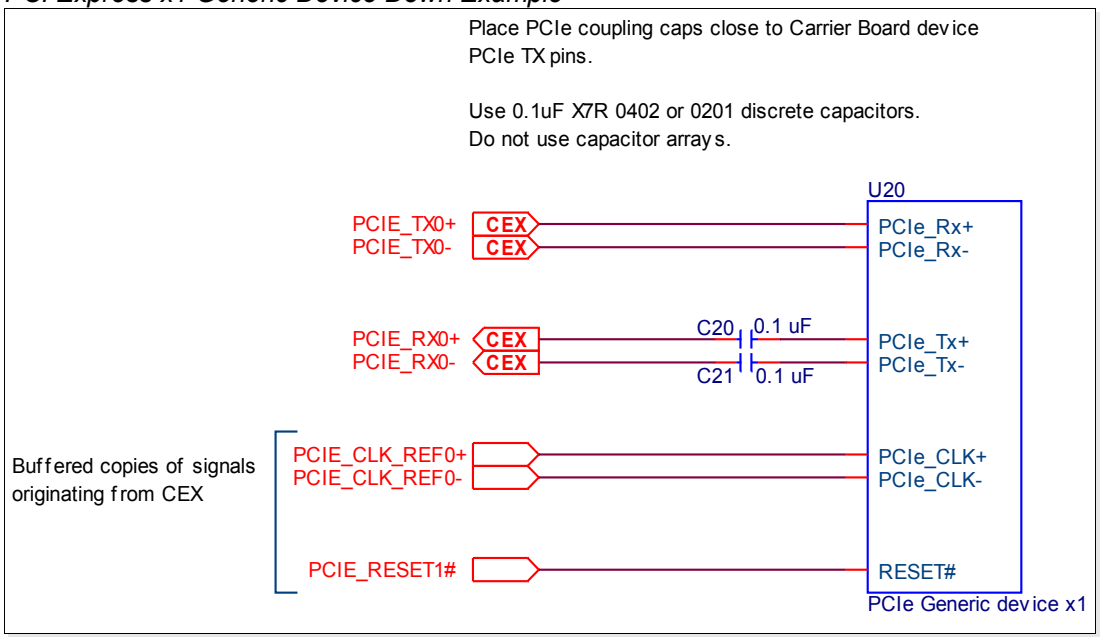
2.3.5.4. x4 Slot Example

Figure 6: PCI Express x4 Slot Example



2.3.5.5. PCIe x1 Generic Device Down Example

Figure 7: PCI Express x1 Generic Device Down Example



A generic example of a PCIe x1 device on a COM Express Carrier Board is shown in the figure above. Only the signals that interface to the COM Express Module in the full power-on state (S0) are shown here.

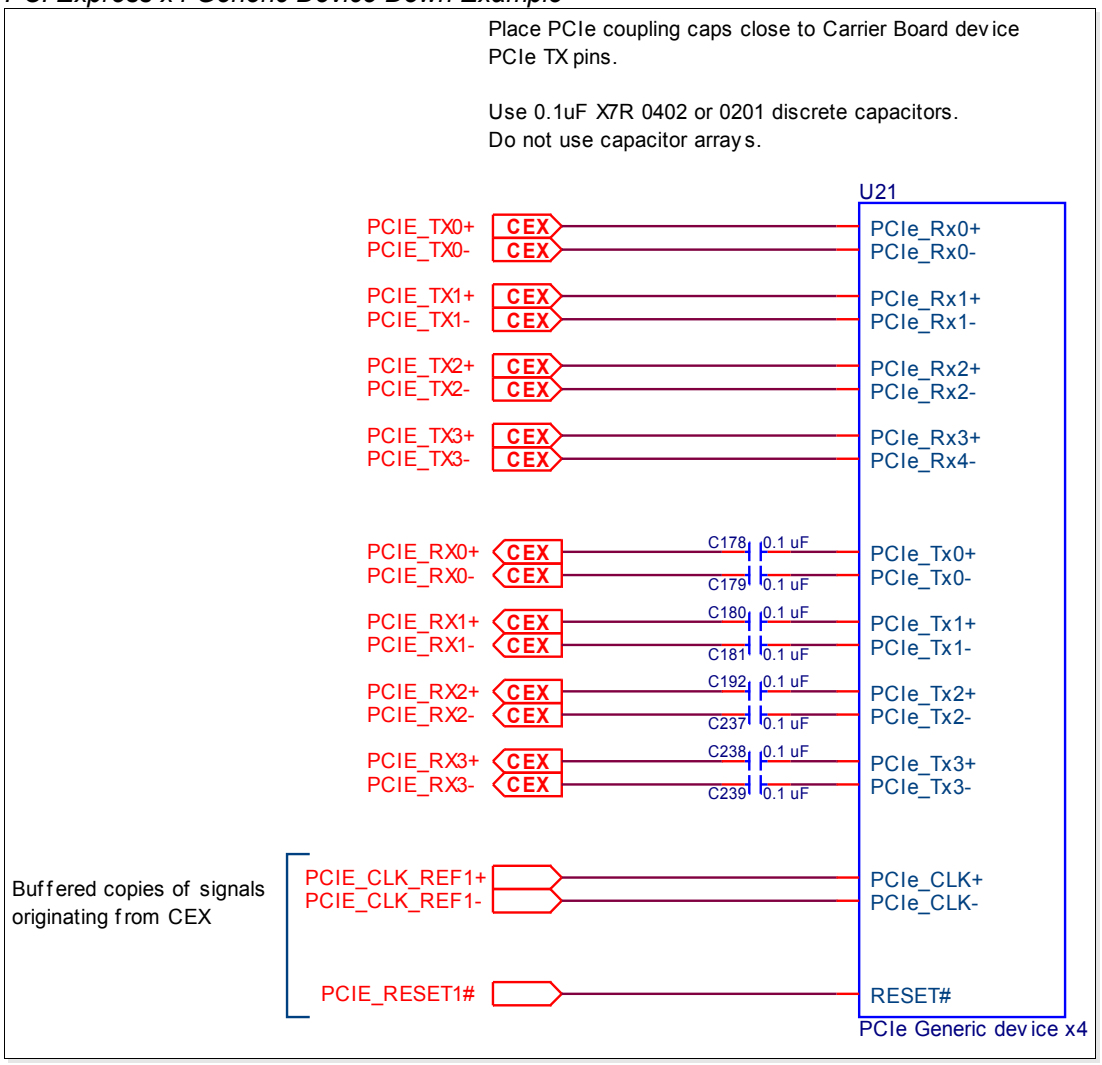
If the Carrier Board device is to support power management features, then some additional signals may come into play. To support wake-up from Suspend states, the Carrier Board device may assert the COM Express WAKE0# input by driving it low through an open drain device.

Some power managed Carrier Board PCIe devices may also have a CLKREQ# signal to disable the PCIe reference clock during periods of inactivity. There is no COM Express destination for this line. It may be used with certain clock buffers – see Figure 4 'PCIe Reference Clock Buffer' on page 22.

Carrier Board PCIe devices may also require SMBUS support. If the Carrier Board device has a Suspend power rail and if its SMBUS pins use that rail, then the device's SMBUS pins may be routed directly to the corresponding COM Express SMBUS pins (SMB_CK, SMB_DAT and SMB_ALERT#). If the Carrier Board SMBUS pins are not powered by the Suspend rail, they must be isolated from the COM Express SMBUS lines by isolation FETs or bus switches. Refer to Section 2.17 'System Management Bus (SMBus)' on page 100 for details.

2.3.5.6. PCIe x4 Generic Device Down Example

Figure 8: PCI Express x4 Generic Device Down Example



A generic example of a PCIe x4 device on a COM Express Carrier Board is shown in the figure above. Only the signals that interface to the COM Express Module in the full power-on state (S0) are shown here.

If the Carrier Board device is to support power management features, then some additional signals may come into play. To support wake-up from Suspend states, the Carrier Board device may assert the COM Express WAKE0# input by driving it low through an open drain device.

Some power managed Carrier Board PCIe devices may also have a CLKREQ# signal to disable the PCIe reference clock during periods of inactivity. There is no COM Express destination for this line. It may be used with certain clock buffers – see Figure 4 'PCIe Reference Clock Buffer' on page 22 above.

Carrier Board PCIe devices may also require SMBUS support. If the Carrier Board device has a Suspend power rail and if its SMBUS pins use that rail, then the device's SMBUS pins may be routed directly to the corresponding COM Express SMBUS pins (SMB_CK, SMB_DAT and SMB_ALERT#). If the Carrier Board SMBUS pins are not powered by the Suspend rail, they must be isolated from the COM Express SMBUS lines by isolation FETs or bus switches. Refer to Section 2.17 'System Management Bus (SMBus)' on page 100 for details.

2.3.5.7. PCI Express Mini Card

The PCI Express Mini Card is a small form factor add-in card optimized for mobile computing and embedded platforms. It is not hot-swappable (for hot swap capability, use an ExpressCard interface, described in Section 2.3.5.8. 'ExpressCard' on page 29 below).

PCI Express Mini Cards are popular for implementing features such as wireless LAN. A small footprint connector can be implemented on the Carrier Board providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradeable, standardized PCI Express Mini Card device to the Carrier Board without additional expenditure of a redesign.

A PCI Express Mini Card interface includes a single x1 PCIe link and a single USB 2.0 channel. The mini PCI Express Card host should offer both interfaces. The PCI Express Mini Card installed into the socket may use either interface.

The source specification for mini-PCI Express Cards is the ***PCI Express Mini Card Electromechanical Specification.***

Figure 9: PCI Express Mini Card Footprint

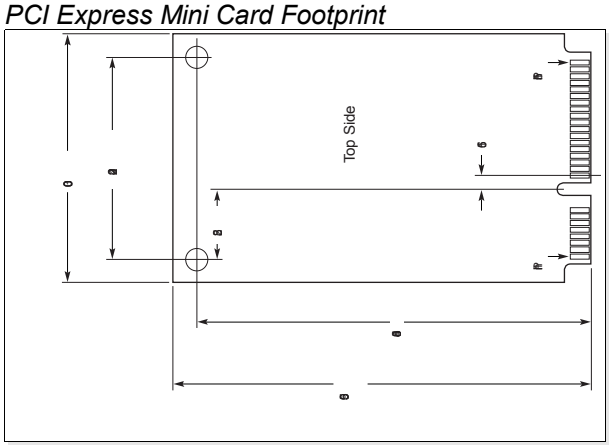
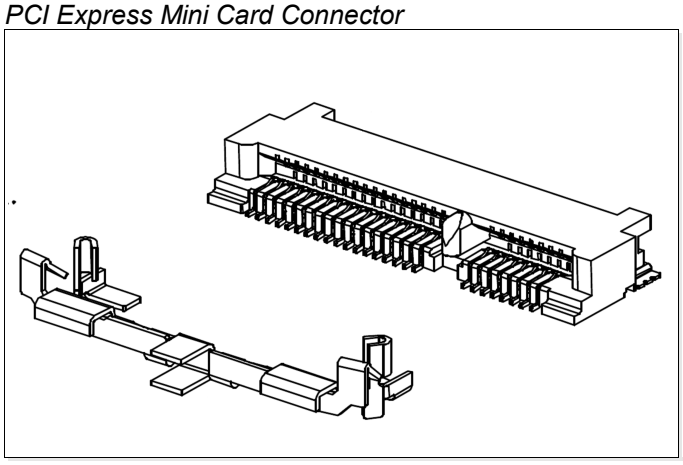


Figure 10: PCI Express Mini Card Connector



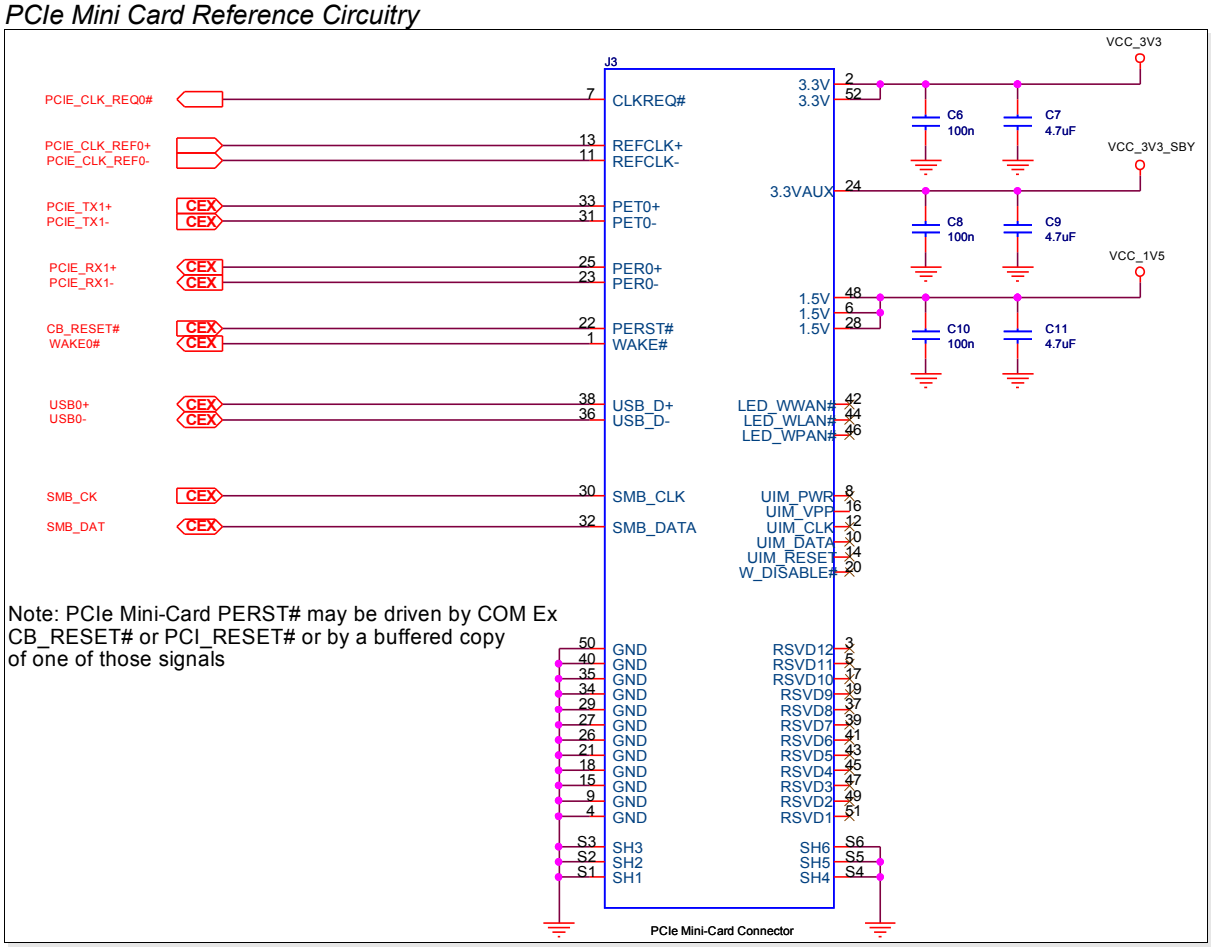
A typical PCI Express Mini-Card socket is shown in Figure 10 above.

The pins used on a PCI Express Mini-Card socket are listed below.

Table 5: PCIe Mini Card Connector Pin-out

Pin	Signal	Description	Pin	Signal	Description
1	WAKE#	Requests the host interface to return to full operation and respond to PCIe.	2	+3.3V	Primary voltage source, 3.3V.
3	RSVD	Reserved	4	GND	Ground
5	RSVD	Reserved	6	+1.5V	Secondary voltage source, 1.5V.
7	CLKREQ#	Reference clock request signal.	8	UIM_PWR	Power source for User Identity Modules (UIM).
9	GND	Ground	10	UIM_DATA	Data signal for UIM.
11	REFCLK-	Reference Clock differential pair negative signal.	12	UIM_CLK	Clock signal for UIM.
13	REFCLK+	Reference Clock differential pair positive signal.	14	UIM_RESET	Reset signal for UIM.
15	GND	Ground	16	UIM_VPP	Variable supply voltage for UIM.
Mechanical Key					
17	RSVD	Reserved for future second User Identity Modules interface (UIM_C8).	18	GND	Ground
19	RSVD	Reserved for future second User Identity Module interface (UIM_C4).	20	W_DISABLE	Used by the system to disable radio operation on add-in cards that implement radio frequency application.
21	GND	Ground	22	PERST#	PCI Express Reset
23	PERn0	Receiver differential pair negative signal, Lane 0.	24	3.3Vaux	Auxiliary voltage source, 3.3V.
25	PERp0	Receiver differential pair positive signal, Lane 0.	26	GND	Ground
27	GND	Ground	28	+1.5V	Secondary voltage source, 1.5V.
29	GND	Ground	30	SMB_CLK	System Management Bus Clock.
31	PETn0	Transmitter differential pair negative signal, Lane 0.	32	SMB_DATA	System Management Bus Data.
33	PETp0	Transmitter differential pair positive Signal, Lane 0.	34	GND	Ground
35	GND	Ground	36	USB_D-	USB Serial Data Interface differential pair, negative signal.
37	RSVD	Reserved for future second PCIe lane.	38	USB_D+	USB Serial Data Interface differential pair, positive signal.
39	RSVD	Reserved for future second PCIe lane.	40	GND	Ground
41	RSVD	Reserved for future second PCIe lane.	42	LED_WWAN#	LED status indicator signals provided by the system.
43	RSVD	Reserved for future second PCIe lane.	44	LED_WLAN#	LED status indicator signals provided by the system.
45	RSVD	Reserved for future second PCIe lane.	46	LED_WPAN#	LED status indicator signals provided by the system.
47	RSVD	Reserved for future second PCIe lane.	48	+1.5V	Secondary voltage source, 1.5V.
49	RSVD	Reserved for future second PCIe lane.	50	GND	Ground
51	RSVD	Reserved for future second PCIe lane.	52	+3.3V	Primary voltage source, 3.3V.

Figure 11: PCIe Mini Card Reference Circuitry



A PCI Express Mini Card schematic example is shown in Figure 11 above. The reference clock pair is sourced from the zero delay clock buffer shown earlier in Figure 4 'PCIe Reference Clock Buffer' on page 22 above. The clock pair is enabled when the PCI Express Mini-Card pulls its CLKREQ# pin low.

The example shows COM Express PCIe lane 1 and USB port 0 used, but other assignments may be made depending on Module capabilities and the system configuration.

If Suspend mode operation is not required, then the 3.3VAUX pin may be tied to VCC_3V3. The WAKE# pin should be left open in this case.

The PERST# pin may be driven by COM Express CB_RESET# or PCI_RESET#, or by buffered copies of the same.

2.3.5.8. ExpressCard

ExpressCards are small form factor hot-swappable peripheral cards designed primarily for mobile computing. The card's electrical interface is through either a x1 PCIe link or a USB 2.0 link. Per the ExpressCard source specification, the host interface should support both the PCIe and USB links. The ExpressCard device may utilize one or the other or both interfaces.

There are several form factors defined, including: 34mm x 75mm; 54mm x 75mm; 34mm x 100mm, and 54mm x 100mm. All of the form factors use the same electrical and physical socket interface.

ExpressCards are the successor to Card Bus Cards (which are PCI-based). Card Bus cards, in turn, are the successors to PCMCIA cards. All three formats are defined by the PCMCIA Consortium.

The source specification document for ExpressCards is the ***ExpressCard Standard.***

COM Express includes four signals that are designated for the support of two ExpressCard slots:

Table 6: Support Signals for ExpressCard

Signal	Pin	Description	I/O
EXCD0_CPPE#	A49	ExpressCard capable card request, slot 0.	I 3.3V CMOS
EXCD1_CPPE#	B48	ExpressCard capable card request, slot 1.	I 3.3V CMOS
EXCD0_PERST#	A48	ExpressCard reset, slot 0.	O 3.3V CMOS
EXCD1_PERST#	B47	ExpressCard reset, slot 1.	O 3.3V CMOS

Figure 12: ExpressCard Size

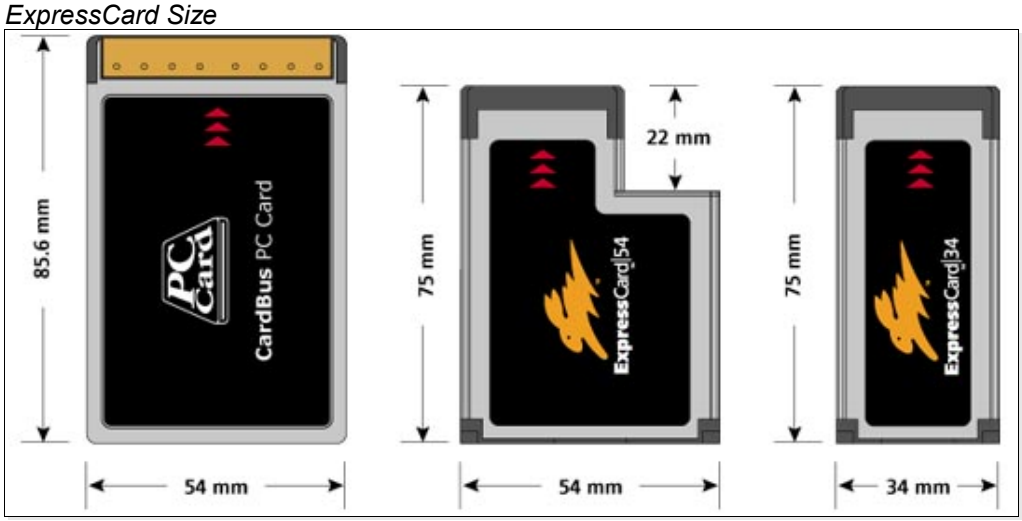


Figure 13: ExpressCard Sockets

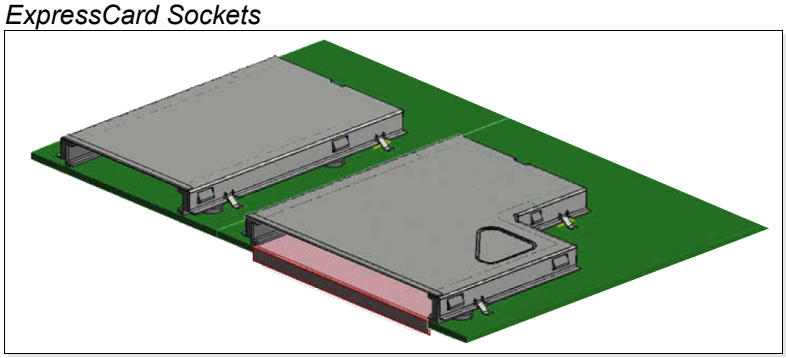


Figure 14: PCI Express: ExpressCard Example

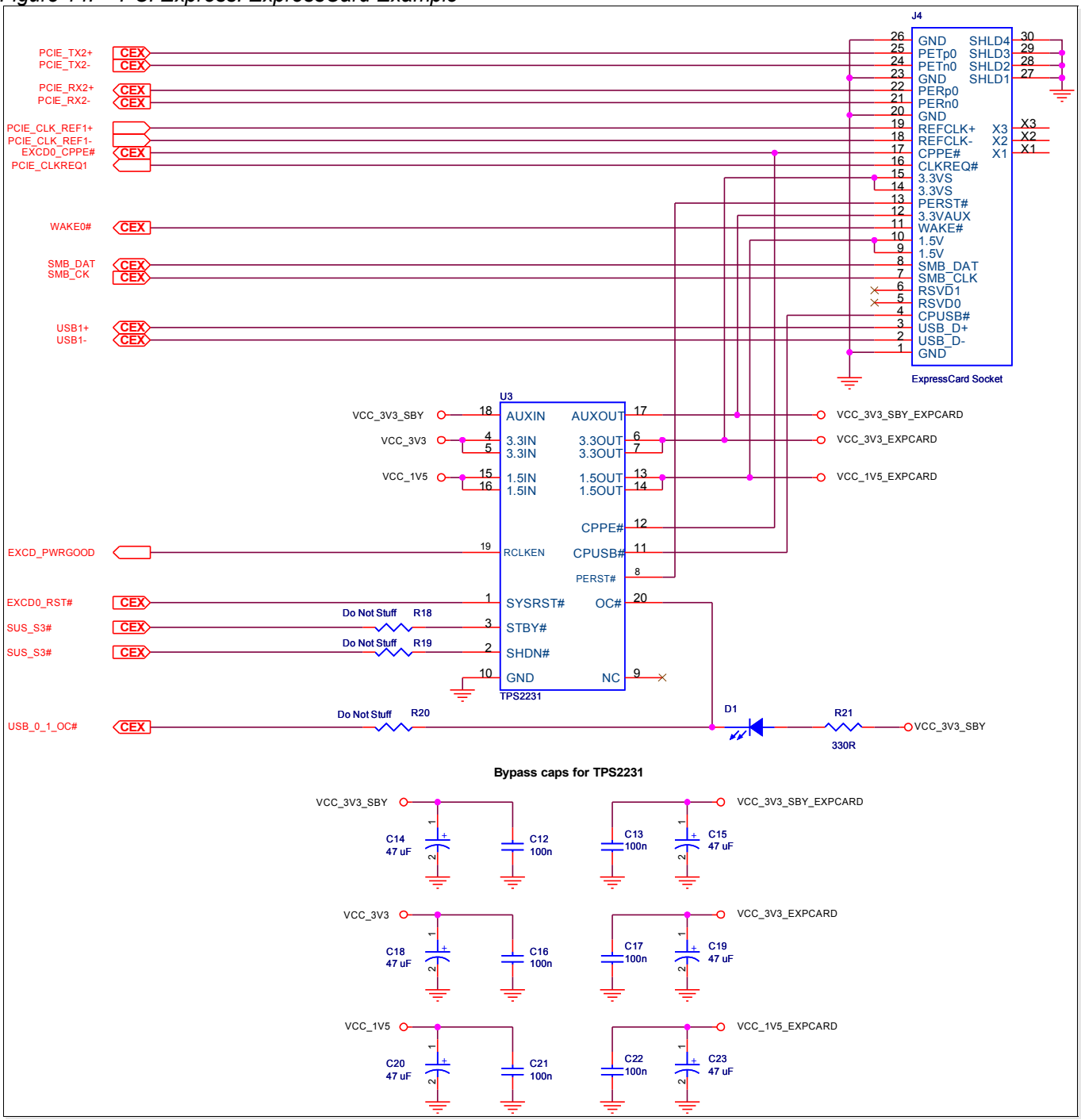


Figure 14 above shows an ExpressCard implementation. The example shows COM Express PCIe lane 2 and USB port 1 used, but other assignments may be made depending on Module capabilities and the system configuration.

Nets PCIE_TX2+ and PCIE_TX2- are sourced from the COM Express Module. These lines drive the PCIe receivers on the Express Card. No coupling capacitors are required on the Carrier Board. These lines are capacitively coupled on the COM Express Module.

Nets PCIE_RX2+ and PCIE_RX2- are driven by the Express Card. No coupling capacitors are required on the Carrier Board. These lines are capacitively coupled on the Express Card.

Nets PCIE_REF_CLK1+ and PCIE_REF_CLK1- are sourced from the PCIe Reference Clock Buffer (described earlier in Section 2.3.5.1. 'Reference Clock Buffer' on page 21 above).

CPPE# is pulled low on the Express Card to indicate that a card is present and has a PCIe interface. CPUSB# is pulled low on the Express Card to indicate the presences of an Express Card and a USB 2.0 interface. Either CPPE# or CPUSB# low causes the TPS2231 ExpressCard power control IC to provide power to the Express Card.

The TPS2231 includes a number of integrated pull-up resistors. Other solutions may require external pull-ups not shown in this schematic example.

CLKREQ# is used for dynamic-clock management. When the signal is pulled low, the dynamic-clock management feature is not supported.

The ExpressCard PCIe reset signal, PERST#, is driven by the TPS2231. PERST# is asserted if the power rails are out of spec or if the COM Express ExpressCard reset, EXCD0_PERST#, is asserted.

WAKE# is asserted by the Express Card to cause the COM Express Module to wake-up at COM Express Module pin B66 WAKE0#. WAKE0# is pulled up on the Module to facilitate the “wire-ORed” interconnect from other WAKE0# sources.

SMB_CK and SMB_DAT are sourced from COM Express Module pins B13 and B14 respectively. The SMBUS supports client-alerting, wireless RF management, and sideband management. Support for the SMBUS is optional on the Carrier Board and the Express Card.

2.3.6. PCI Express Routing Considerations

PCI Express (PCIe) signals are high-speed differential pairs with a nominal 100Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

PCIe pairs need to be length-matched within a given pair (“intra-pair”), but the different pairs do not need to be closely matched (“inter-pair”).

PCB design rules for these signals are summarized in Section 6. 'Carrier Board PCB Layout Guidelines' on page 126.

2.3.6.1. Polarity Inversion

Per the ***PCI Express Card Electromechanical Specification***, all PCIe devices must support polarity inversion on each PCIe lane, independently of the other lanes. This means that, for example, you can route the Module PCIE_TX0+ signal to the corresponding ‘-’ pin on the slot or target device, and the PCIE_TX0- signal to the corresponding ‘+’ pin. If this makes the layout cleaner, with fewer layer transitions and better differential pairs, then take advantage of this PCIe feature.

2.3.6.2. Lane Reversal

PCIe lane reversal is not supported on the COM Express general purpose PCIe lanes. For x1 links, lane reversal is not relevant. It would potentially be useful for a x4 link, but is not supported in the COM Express specification. It is also not supported by the current crop of South Bridge chip-set components commonly used to create the general purpose PCIe lanes on COM Express Modules.

Lane reversal is supported for the COM Express x16 PEG interface. See Section 2.4. 'PEG (PCI Express Graphics)' on page 33 for details.

2.4. PEG (PCI Express Graphics)

2.4.1. Signal Definitions

The PEG Port can utilize COM Express PCIe lanes 16-32 and is suitable to drive a x16 link for an external high-performance PCI Express Graphics card, if implemented on the COM Express module. It supports a theoretical bandwidth of up to 4 GB/s – twice the peak bandwidth achievable with AGP 8x. Each lane of the PEG Port consists of a receive and transmit differential signal pair designated 'PEG_RX0' (+ and -) to 'PEG_RX15' (+ and -) and correspondingly from 'PEG_TX0' (+ and -) to 'PEG_TX15' (+ and -). The corresponding signals can be found on the Module connector rows C and D.

The pins of the PEG Port might be shared with other functionality like SDVO or DVO, depending on the chipset used. SDVO and PEG are defined on COM Express specification as “may be used”. Please be sure the functionality you require is supported by your module vendor.

Table 7: PEG Signal Description

Signal	Pin#	Description	I/O	Comment
PEG_RX0+ PEG_RX0-	C52 C53	PEG channel 0, Receive Input differential pair.	I PCIE	Shared with: SDVO_TVCLKIN+ SDVO_TVCLKIN-
PEG_TX0+ PEG_TX0-	D52 D53	PEG channel 0, Transmit Output differential pair.	O PCIE	Shared with: SDVOB_RED+ SDVOB_RED-
PEG_RX1+ PEG_RX1-	C55 C56	PEG channel 1, Receive Input differential pair.	I PCIE	Shared with: SDVOB_INT+ SDVOB_INT-
PEG_TX1+ PEG_TX1-	D55 D56	PEG channel 1, Transmit Output differential pair.	O PCIE	Shared with: SDVOB_GRN+ SDVOB_GRN-
PEG_RX2+ PEG_RX2-	C58 C59	PEG channel 2, Receive Input differential pair.	I PCIE	Shared with: SDVO_FLDSTALL+ SDVO_FLDSTALL-
PEG_TX2+ PEG_TX2-	D58 D59	PEG channel 2, Transmit Output differential pair.	O PCIE	Shared with: SDVOB_BLU+ SDVOB_BLU-
PEG_RX3+ PEG_RX3-	C61 C62	PEG channel 3, Receive Input differential pair.	I PCIE	
PEG_TX3+ PEG_TX3-	D61 D62	PEG channel 3, Transmit Output differential pair.	O PCIE	Shared with: SDVOB_CK+ SDVOB_CK-
PEG_RX4+ PEG_RX4-	C65 C66	PEG channel 4, Receive Input differential pair.	I PCIE	
PEG_TX4+ PEG_TX4-	D65 D66	PEG channel 4, Transmit Output differential pair.	O PCIE	Shared with: SDVOC_RED+ SDVOC_RED-
PEG_RX5+ PEG_RX5-	C68 C69	PEG channel 5, Receive Input differential pair.	I PCIE	Shared with: SDVOC_INT+ SDVOC_INT-
PEG_TX5+ PEG_TX5-	D68 D69	PEG channel 5, Transmit Output differential pair.	O PCIE	Shared with: SDVOC_GRN+ SDVOC_GRN-
PEG_RX6+ PEG_RX6-	C71 C72	PEG channel 6, Receive Input differential pair.	I PCIE	
PEG_TX6+ PEG_TX6-	D71 D72	PEG channel 6, Transmit Output differential pair.	O PCIE	Shared with: SDVOC_BLU+ SDVOC_BLU-
PEG_RX7+ PEG_RX7-	C74 C75	PEG channel 7, Receive Input differential pair.	I PCIE	
PEG_TX7+ PEG_TX7-	D74 D75	PEG channel 7, Transmit Output differential pair.	O PCIE	Shared with: SDVOC_CK+ SDVOC_CK-
PEG_RX8+ PEG_RX8-	C78 C79	PEG channel 8, Receive Input differential pair.	I PCIE	
PEG_TX8+ PEG_TX8-	D78 D79	PEG channel 8, Transmit Output differential pair.	O PCIE	
PEG_RX9+ PEG_RX9-	C81 C82	PEG channel 9, Receive Input differential pair.	I PCIE	

Signal	Pin#	Description	I/O	Comment
PEG_TX9+ PEG_TX9-	D81 D82	PEG channel 9, Transmit Output differential pair.	O PCIE	
PEG_RX10+ PEG_RX10-	C85 C86	PEG channel 10, Receive Input differential pair.	I PCIE	
PEG_TX10+ PEG_TX10-	D85 D86	PEG channel 10, Transmit Output differential pair.	O PCIE	
PEG_RX11+ PEG_RX11-	C88 C89	PEG channel 11, Receive Input differential pair.	I PCIE	
PEG_TX11+ PEG_TX11-	D88 D89	PEG channel 11, Transmit Output differential pair.	O PCIE	
PEG_RX12+ PEG_RX12-	C91 C92	PEG channel 12, Receive Input differential pair.	I PCIE	
PEG_TX12+ PEG_TX12-	D91 D92	PEG channel 12, Transmit Output differential pair.	O PCIE	
PEG_RX13+ PEG_RX13-	C94 C95	PEG channel 13, Receive Input differential pair.	I PCIE	
PEG_TX13+ PEG_TX13-	D94 D95	PEG channel 13 Transmit Output differential pair.	O PCIE	
PEG_RX14+ PEG_RX14-	C98 C99	PEG channel 5, Receive Input differential pair.	I PCIE	
PEG_TX14+ PEG_TX14-	D98 D99	PEG channel 5, Transmit Output differential pair.	O PCIE	
PEG_RX15+ PEG_RX15-	C101 C102	PEG channel 5, Receive Input differential pair.	I PCIE	
PEG_TX15+ PEG_TX15-	D101 D102	PEG channel 5, Transmit Output differential pair.	O PCIE	
SDVO_I2C_CLK	D73	I2C based control signal (clock) for SDVO device.	O 2.5V CMOS	SDVO enabled if this line is pulled up to 2.5V on Carrier or on ADD2
SDVO_I2C_DATA	C73	I2C based control signal (data) for SDVO device	I/O 2.5V OD CMOS	SDVO enabled if this line is pulled up to 2.5V on Carrier or on ADD2
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 3.3V CMOS	
PEG_ENABLE#	D97	PEG enable function. Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	I 3.3V CMOS	
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes	O CMOS	COM Express only allocates a single reference clock

2.4.2. PEG Configuration

The COM Express PCIe Graphics (PEG) Port is comprised of COM Express PCIe lanes 16-32. The primary use of this set of signals is to interface to off-Module graphics controllers or cards. The COM Express spec also allows these pins to be shared with a set of Module generated SDVO lines.

If the PEG interface is not used for an external graphics card or SDVO, it may be possible to use these PCIe lanes for other Carrier Board PCIe devices. The details of this usage are Module and Module chip-set dependent. Operation in a x1 link is also supported. Wider links (x2, x4, x8, x16) are chip-set dependent. Refer to the Module product documentation for details.

The COM Express specification defines a fill order for this set of PCIe lanes. Larger link widths go to the lower lanes. Refer to the COM Express specification for details.

2.4.2.1. Using PEG Pins for an External Graphics Card

To use the COM Express PEG lanes for an external graphics device or card, the Module PEG_ENABLE# line (pin D97 on the Module C-D connector) must be pulled low. Pulling this pin low disables the Module's internal graphics controller and makes the PEG x16 interface available to an external controller.

The usual effect of pulling PEG_ENABLE# low is to disable the on-Module graphics engine. For some Modules, it is possible to configure the Module such that the internal graphics engine remains active, even when the external PEG interface is being used for a Carrier Board graphics device. This is Module dependent. Check with your vendor.

If the external graphics controller is “down” on the Carrier Board, then the PEG_ENABLE# line should be pulled to GND on the Carrier Board.

There are four copies of PRSNT2# defined for slot cards, to allow detection of x1, x4, x8 and x16 cards. For PEG slot use, the PRSNT2# signals for the x1 and x4 links are used for SDVO detection per the following chart.

To enable carrier flexibility in slot configuration and to support x1, x4, x8 and x16 PCI Express cards as well as ADD2/MEC cards and MEC cards that utilize both SDVO and x1 PCI Express, a jumper is recommended on the carrier to configure the PEG_ENABLE# signal. For carrier implementations only requiring support of x8 and x16 PCI Express graphics cards and SDVO ADD2 cards, the PRSNT2# signals on slot pins B48 and B81 may be tied to COM Express Module PEG_ENABLE# pin D97 to automatically configure the module based on the card inserted.

Table 8: PEG Configuration Pins

Slot Signal	Slot Pin	Carrier Board Connection	COM Ex Pin	Comment
PRSNT1#	A1	Tie to GND through low value resistor		Pins A1, B48 and B81 are tied together on a PEG slot card. Not tied together on ADD2.
PRSNT2#	B17	To COM Ex SDVO_I2C_CLK line	D73	SDVO use – pulled to 2.5V on ADD2
PRSNT2#	B31	To COM Ex SDVO_I2C_DAT line	C73	SDVO use – pulled to 2.5V on ADD2
PRSNT2#	B48	Not connected		
PRSNT2#	B81	To COM Ex PEG_ENABLE#Not connected		

2.4.2.2. Using PEG Pins for SDVO

The COM Express Module graphics controller configures the PEG lines for SDVO operation if it detects that COM Express signals SDVO_I2C_CLK and SDVO_I2C_DATA are pulled high to 2.5V, and if the PEG_ENABLE# line is left floating. This combination leaves the Module's internal graphics engine enabled but converts the output format to SDVO. The SDVO_I2C_CLK and SDVO_I2C_DATA lines are pulled to 2.5V on an ADD2 card.

For a device “down” SDVO converter, the SDVO_I2C_CLK and SDVO_I2C_DATA lines have to be pulled up to 2.5V on the Carrier Board.

2.4.2.3. Using PEG Pins for General Purpose PCIe Lanes

The COM Express PEG lanes may be used for general-purpose use if the PEG port is not being used as an interface to an external graphics device. The characteristics of this usage are Module and chip-set dependent.

Modules that employ desktop and mobile chip-sets with PEG capability can usually be set up to allow the COM Express PEG lanes to be configured as a single general purpose PCIe link, with link width possibilities of x1, x4, x8 or x16. The x1 configuration should always work; the wider links may be Module and chip-set dependent. Check with your vendor.

Modules based on server-class chip-sets may allow multiple links over the PEG lanes – for example, a x8 link on COM Express PCIe lanes 16 through 23 and a x4 link over lanes 24 through 27. This is Module and chip-set dependent.

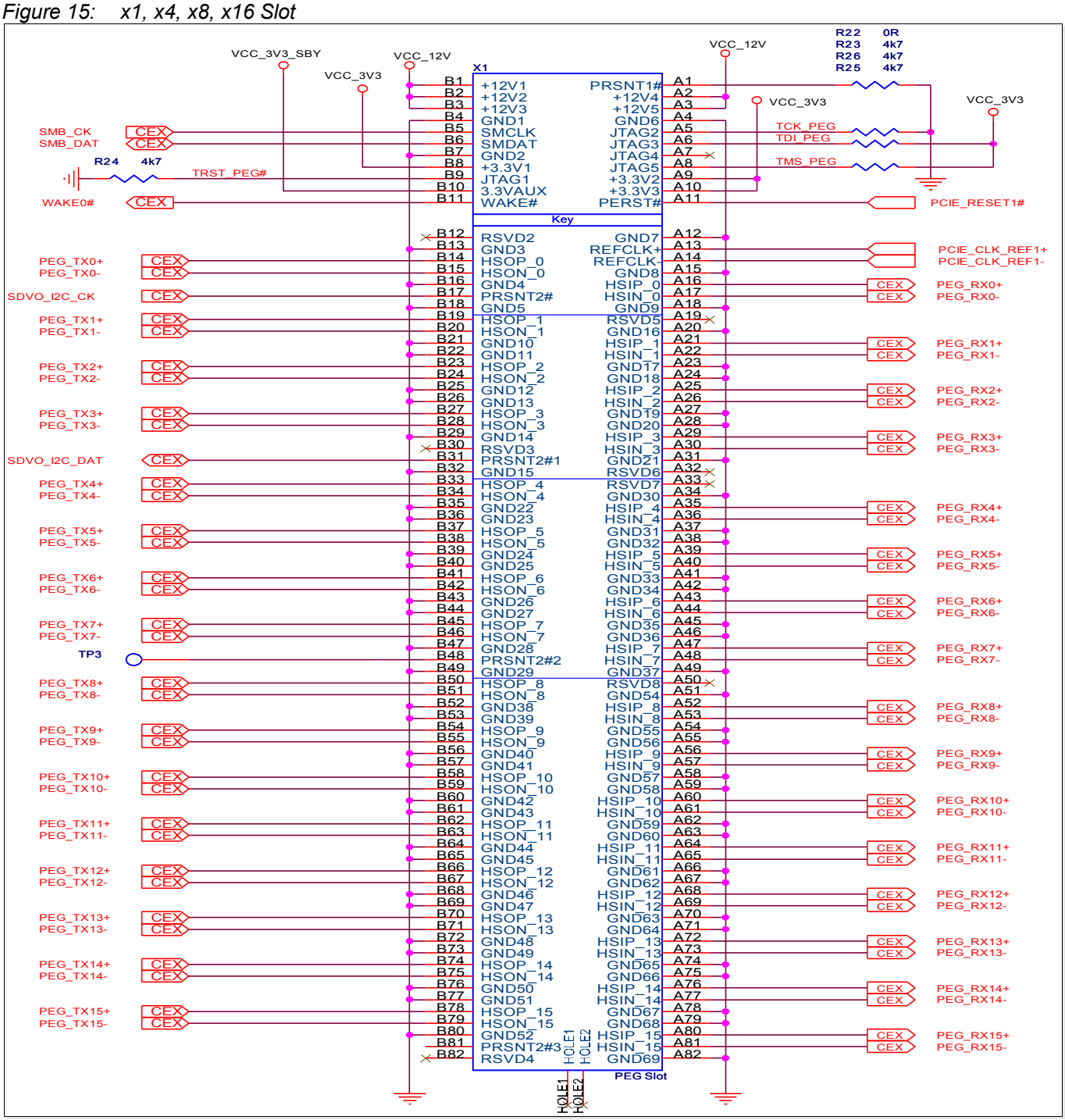
PEG_ENABLE# should be left open when the PEG lanes are to be used for general purpose PCIe links.

2.4.3. Reference Schematics

2.4.3.1. x1, x4, x8, x16 Slot

Figure 15 below illustrates the pinout definition for the standard x1, x4, x8 and x16 PCI Express connectors. The dashed lines in the diagram depict where each different connector type ends.

Figure 15: x1, x4, x8, x16 Slot



The x16 connector usually is used to drive the PCI Express Graphics Port (PEG) consisting of 16 PEG lanes, which are connected to the appropriate x16 connector pins. For more information about the signal definition of the PEG port, refer to Section 2.4. 'PEG (PCI Express Graphics)' on page 33 above.

Note: Auxiliary signals
The auxiliary signals are provided on the PCI Express connectors to assist with certain system level functionality or implementations. Some of these signals are required when implementing a PCI connector on the Carrier Board. For more information about this subject, refer to the PCI Express Card Electromechanical Specification, Rev. 1.1 Section 2.

2.4.4. Routing Considerations

PCI Express (PCIe) signals are high-speed differential pairs with a nominal 100Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

PCIe pairs need to be length-matched within a given pair (“intra-pair”), but the different pairs do not need to be closely matched (“inter-pair”).

PCB design rules for these signals are summarized in Section 6 'Carrier Board PCB Layout Guidelines' starting on page 126.

2.4.4.1. Polarity Inversion

Per definition, PCI Express supports polarity inversion by each receiver on a link. The receiver accomplishes this by simply inverting the received data on the differential pair if it detects a polarity inversion during the initial training sequence of the link. In other words, a lane will still work correctly if a positive signal 'PEG_TX+' from a transmitter is connected to the negative signal 'PEG_RX-' of the receiver. Vice versa, the negative signal from the transmitter 'PEG_TX-' must be connected to the positive signal of the receiver 'PEG_RX+'. This feature can be very useful to make PCB layouts cleaner and easier to route.

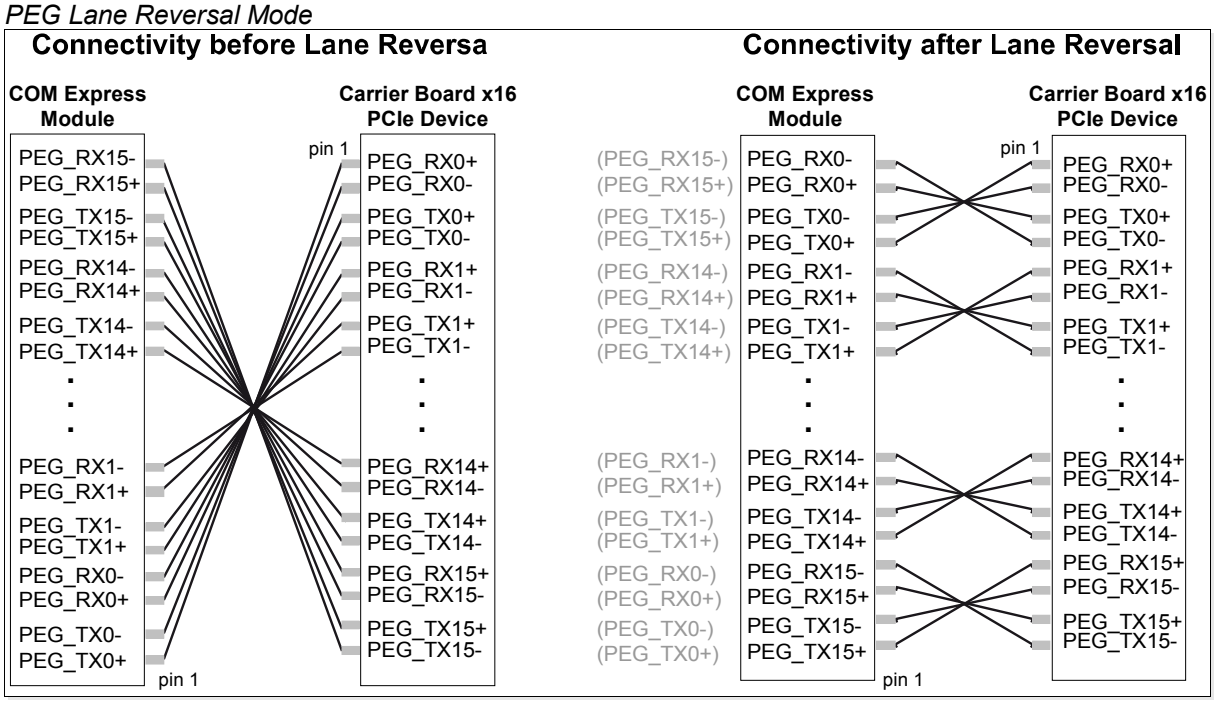
Polarity inversion does not imply direction inversion, this means the 'PEG_TX' differential pairs of the Module must still be connected to the 'PEG_RX' differential signal pairs of the device.

2.4.4.2. Lane Reversal

During the PCB layout of a COM Express Carrier Board, it is quite possible that the signals between the Modules connectors and the PCI Express device on the Carrier Board have to be crossed. To help layout designers overcome this signal crossing scenario, PCI Express specifies Lane Reversal. Lane Reversal is the reverse mapping of lanes for x2 or greater links.

For example, on a link with a width of x16, which supports Lane Reversal, the TX0, TX1, ... TX14, TX15 of the transmitting device have to be connected to RX15, RX14, ... RX1, RX0 of the receiving device, and vice versa. See Figure 16 below.

Figure 16: PEG Lane Reversal Mode



To activate the Lane Reversal mode for the PEG Port, the COM Express specification defines an active low signal 'PEG_LANE_RV#', which can be found on the Modules connector at row D pin D54. This pin is strapped low on the Carrier Board to invoke Lane Reversal mode.

Note ***Please be aware that the SDVO lines (Section 2.5) that share the PEG Port (Section 2.4) may not support Lane Reversal mode. This is the reason that there are "normal" (ADD2-N) and "reverse" (ADD2-R) pin-out ADD2 cards on the market. ADD2-N cards are used in a PEG slot that does not employ lane reversal. An ADD2-R card is used in a PEG slot that does employ lane reversal.***

Check with your Module vendor to see if SDVO Lane Reversal is supported. Modules based on Intel 915 chip-sets generally do not support SDVO Lane Reversal. Modules based on Intel 945 and 965 chip-sets generally do support it.

2.5. SDVO

SDVO was developed by the Intel® Corporation to interface third party SDVO compliant display controller devices that may have a variety of output formats, including DVI, LVDS, HDMI and TV-Out. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependent upon the active display resolution and timing.

2.5.1. Signal Definitions

The pins for SDVO ports B and C are shared with the PEG port. The SDVO interface of the COM Express module features its own dedicated I²C bus (SDVO_I2C_CLK and SDVO_I2C_DAT). It is used to control the external SDVO devices and to read out the display timing data from the connected display.

The COM Express Module graphics controller configures the PEG lines for SDVO operation if it detects that COM Express signals SDVO_I2C_CLK and SDVO_I2C_DATA are pulled high to 2.5V, and if the PEG_ENABLE# line is left floating. This combination leaves the Module's internal graphics engine enabled but converts the output format to SDVO. The SDVO_I2C_CLK and SDVO_I2C_DATA lines are pulled to 2.5V on an ADD2 card.

For a device “down” SDVO converter, the SDVO_I2C_CLK and SDVO_I2C_DATA lines have to be pulled up to 2.5V on the Carrier Board and PEG_ENABLE# left open.

2.5.1.1. SDVO Port Configuration

The SDVO port and device configuration is fixed within the Intel® Graphics Video BIOS implementation of the COM Express module. All COM Express modules assume a I²C bus address 1110 000x for SDVO devices connected to port B and an I²C bus address of 1110 010x for SDVO devices connected to port C. Table 9 below lists the supported SDVO port configurations.

Table 9: SDVO Port Configuration

	SDVO Port B	SDVO Port C
Device Type	Selectable in BIOS Setup Program.	Selectable in BIOS Setup Program.
I²C Address	1110 000x	1110 010x
I²C Bus	SDVO I²C GPIO pins	SDVO I²C GPIO pins
DDC Bus	SDVO I²C GPIO pins	SDVO I²C GPIO pins

2.5.1.2. Supported SDVO Devices

Due to the fact that SDVO is an Intel® defined interface, the number of supported SDVO devices is limited to devices that are supported by the Intel® Graphics Video BIOS and Graphics Driver software.

Table 10: Intel® SDVO Supported Device Descriptions

Device	Vendor	Type	Link
CH7021A	Chrontel	SDTV / HDTV	http://www.chrontel.com
CH7308A	Chrontel	LVDS	http://www.chrontel.com
CH7307C	Chrontel	DVI	http://www.chrontel.com
CH7312	Chrontel	DVI	http://www.chrontel.com
CX25905	Conexant	DVI-D / TV / CRT	http://www.conexant.com
SiL1362/1364	Silicon Image	DVI	http://www.siliconimage.com
SiL 1390	Silicon Image	HDMI	http://www.siliconimage.com

Note: The devices listed in Table 10 require BIOS support for proper operation. Check with the modules vendor for a list of specific devices that are supported.

2.5.2. Reference Schematics

2.5.2.1. SDVO to DVI Transmitter Example

Figure 17: SDVO to DVI Transmitter Example

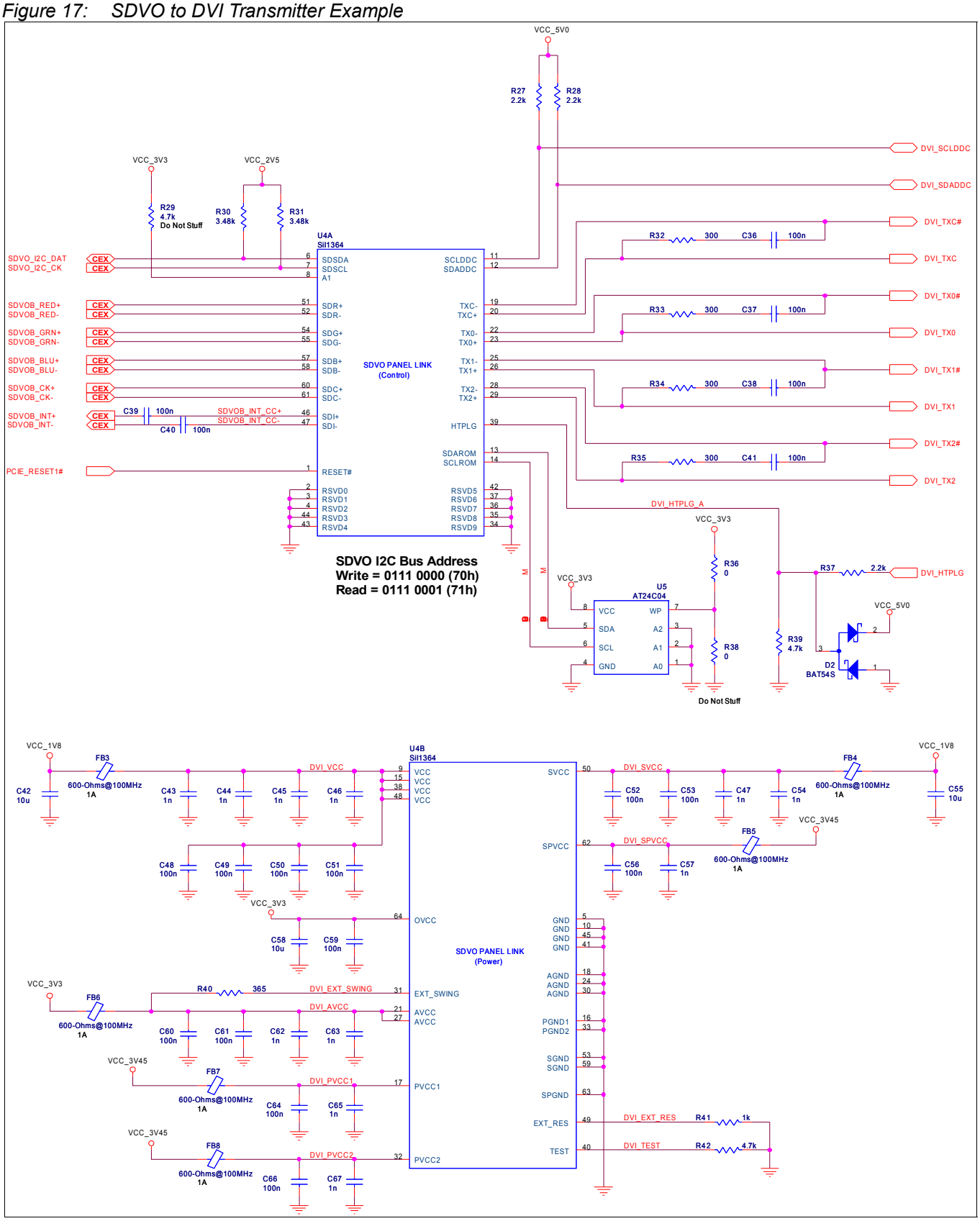


Figure 17 'SDVO to DVI Transmitter Example' above shows a single-channel, device-down application for SDVO to DVI implementation. A Silicon Image transmitter IC (SIL1364) converts SDVO signals from the Module to a DVI-D format. Pins are connected to the DVI-D Connector (Molex 74320-4004).

PEG_RX1+ and PEG_RX1- are sourced from COM Express Module pins C55 and C56 and are defined as SDVOB_INT+ and SDVOB_INT- in the COM Express Specification respectively. They are driven by SDI+ and SDI- from the chip. The PEG Receive interface on the COM Express Module is driven by the TX source (Interrupt) on the SDVO chip. The TX source needs to be AC-coupled near the source (SDI pins).

EXT_RES is pulled low through a 1.0kΩ resistor to generate a reference-bias current.

PEG_TX0+/- through PEG_TX3- from COM Express Module pins are defined as SDVO_RED+/-, GRN+/-, BLU+/- and CK+/- in the COM Express Specification respectively. They drive SDR+/-, SDG+/-, SDB+/- and SDC+/- on the chip. The PEG Transmit interface on the COM Express Module drives the RX load on the graphics chip.

SDVO_I2C_CLK and SDVO_I2C_DAT are sourced from COM Express Module pins D73 and C73 respectively. A pull-up to 2.5V using a 3.5kΩ resistor is required for both lines on the Carrier Board for a device-down application. For an SDVO slot design, pull-ups are on the SDVO plug-in card.

The I2C Bus supports management functions and provides Manufacturer information, a model number, and a part number.

RESET# is driven by the PCI_RESET#_B from COM Express Module pin C23, PCI_RESET#, after buffering. The signal resets the chip and causes initialization.

A1 establishes the I2C default address. Pulled Low = 0X70 (unconnected). Pulled High = 0X72 through a 4.7kΩ resistor.

HTPLUG – The Hot Plug input is driven by the Monitor Device, which causes the System OS to initiate a Plug and Play sequence that results in identifying the configuration of the Monitor. Protection diodes and a current-limiting resistor also are added.

TEST – The factory test pin needs to be tied low for normal operation.

EXT_SWING should be tied to AVCC pins through a 360Ω resistor. It sets the amplitude voltage swing. Smaller values set a larger voltage swing and vice versa.

SDAROM and SCLROM interface to a non-volatile memory U17, Serial Prom AT24C04.

TX0+/- through TX2+/- DVI output pins are TMDS low voltage differential signals.

TXC+/- DVI Clock pins are TMDS low voltage differential signals.

SCLDDC and SDADDC should be pulled up with a 2.2kΩ resistor. They serve as the signals for the I2C interface to the DVI connector. The interface supports the DDC (Display Data Channel) standard for EDID (Extended Display Identification Data) over I2C. The EDID includes the manufacturer’s name, product type, phosphor or filter type, timings supported by the display, display size, luminance data and pixel mapping data (for digital displays only).

SDAROM and SCLROM external pull-ups are not required because they are internally pulled up. They serve as signals for the I2C interface to EEPROM AT24C04.

The schematics also show the requirements for decoupling and the filter caps for the SIL1364 graphics chip.

2.5.2.2. Other SDVO Output Options: LVDS, NTSC

SDVO to LVDS interface chips are available from multiple vendors. One example is the Chrontel CH7308.

SDVO to NTSC interface chips are available from multiple vendors including Chrontel.

Note: Please also follow the design guidelines from the SDVO chip vendor

2.5.3. Routing Considerations

For the SDVO interconnection between the COM Express module and a third-party SDVO compliant device, refer to 6.4.4. 'SDVO Trace Routing Guidelines' on page 135 below and to the layout and routing considerations specified by the SDVO device manufacturer.

The Digital Video Interface (DVI) is based on the differential signaling method TDMS. To achieve the full performance and reliability of DVI, the TDMS differential signals between the SDVO to DVI transmitter and the DVI connector have to be routed in pairs with a differential impedance of 100Ω. The length of the differential signals must be kept as close to the same as possible. The maximum length difference must not exceed 100mils for any of the pairs relative to each other. Spacing between the differential pair traces should be more than 2x the trace width to reduce trace-to-trace couplings. For example, having wider gaps between differential pair DVI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DVI traces on the same layer. There should be a minimum distance of 30mils between the DVI trace and any ground on the same layer. For more information, refer to the layout and routing considerations as specified by the manufacturer of the SDVO to DVI transmitter.

2.5.3.1. SDVO Option – PEG Lane Reversal

If Module pin D54 PEG_LANE_RV# is strapped low to untwist a bowtie on the PEGx16 lines to an x16 slot, then an ADD2 card used in this slot must be a reverse pin-out ADD2 card. Reverse pin-out ADD2 cards are designated ADD2-R.

If the SDVO device is “down” on the Carrier Board, then the PEG_LANE_REV# pin has no effect because SDVO lines are not reversed on the chipset – only PCIe x16 lines are.

Please see the Lane Reversal caution at Section 2.4.4.2. 'Lane Reversal' on page 38 above.

2.6. LAN

All COM Express Modules provide at least one LAN port. The 8-wire 10/100/1000BaseT Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the COM Express Module PHY responsible for implementing autonegotiation of 10/100BaseTX vs 10/100/1000BaseT operation. The carrier may also support a 4-wire 10/100BaseTX interface from the COM Express Module on an exception basis. Check with your vendor for 10/100 only implementations.

2.6.1. Signal Definitions

The LAN interface of the COM Express Module consists of 4 pairs of low voltage differential pair signals designated from *'GBE0_MDI0'* (+ and -) to *'GBE0_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect to a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetics on the Carrier Board. The corresponding LAN differential pair and control signals can be found on rows A and B of the Module's connector, as listed in Table 11 below.

Table 11: LAN Interface Signal Descriptions

Signal	Pin#	Description	I/O	Comment
GBE0_MDI0+ GBE0_MDI0-	A13 A12	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is used for all modes.
GBE0_MDI1+ GBE0_MDI1-	A10 A9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is used for all modes.
GBE0_MDI2+ GBE0_MDI2-	A7 A6	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI3+ GBE0_MDI3-	A3 A2	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	REF	
GBE0_LINK#	A8	Ethernet controller 0 link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_LINK100#	A4	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_LINK1000#	A5	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_ACT#	B2	Ethernet controller 0 activity indicator, active low.	O 3.3V Suspend OD CMOS	

2.6.1.1. Status LED Signal Definitions

The four link status signals (LINK#, LINK100#, LINK1000#, and ACT#) are combined on the carrier to drive two status LEDs (Link Activity and Link Speed). These two LEDs are typically integrated into the RJ45 receptacle housing for the Ethernet, but may be placed on the carrier Module assembly as discrete LEDs. The most common functional characteristics for each LED are listed in Table 12 below.

Table 12: LAN Interface LED Function

LED-Function	LED Color#	LED State	Description
Link Speed	Greed / Orange	Off	10 Mbps link speed
		Green	100 Mbps link speed
		Orange	1000 Mbps link speed
Link Status & Activity	Yellow	Off	No Link
		Steady On	Link established, no activity detected
		Blinking	Link established, activity detected

2.6.1.2. LAN 1 and 2 shared with IDE

The Type 2 COM Express Module only provides one LAN port to the carrier. Type 3 and 5 COM Express Modules provide two additional 10/100/1000BaseT Gigabit Ethernet ports in place of the IDE port, and Type 5 Module definitions include an option to support 10 Gigabit Ethernet port operation.

This Design Guide does not explicitly define Carrier Board support for the Type 3 and 5 COM Express Modules. However, it is recommended that a carrier supporting one of those Modules should follow the guidelines for the LAN 0 port carrier circuit in this section when defining the LAN 1 and 2 port carrier circuits.

2.6.1.3. PHY / Magnetics Connections

The COM Express Module specification partitions the IEEE 802.3 PHY / MDI interface circuit resources between the Module and carrier, with the PHY located on the Module and the coupling magnetics located on the carrier, preferably physically integrated in the RJ-45 receptacle housing associated with the port. Section 5.4.5 of the COM Express Module specification shows this circuit topology and provides a high level signal attenuation budget for Ethernet signals traversing this circuit.

In order to meet the signal performance requirements for MDI signals as defined in the IEEE 802.3-2005 specification and to ensure maximum interoperability of COM Express Modules and carriers, the PHY / Magnetics circuit should be implemented using the following guidelines:

- The carrier should provide a full 8-wire (10/100/1000baseT) interface circuit to the COM Express Module
- The termination resistors should be placed on the COM Express Module, physically as close to the PHY device receive inputs as practical
- The center tap reference signal should be routed from the COM Express Module connector to the secondary side center tap of each transformer as defined in the IEEE 802.3-2005 specification, without any series resistance or impedance circuits
- The Carrier Board design should utilize a coupling transformer capable of interoperating with the largest possible number of PHY devices
- The Carrier Board design should have the primary side and secondary side center tap termination components (75 Ω resistors and 100 nF capacitors, respectively) placed physically as close to the coupling transformer as possible
- The coupling transformer should be placed no further than 100mm (3.9”) from the COM Express Module connector on the Carrier Board.
- It is recommended that the carrier use a RJ-45 connector with an integrated transformer. However, if a discrete coupling transformer is used, the transformer must be placed no further than 25mm (1.0”) from the RJ-45 receptacle.

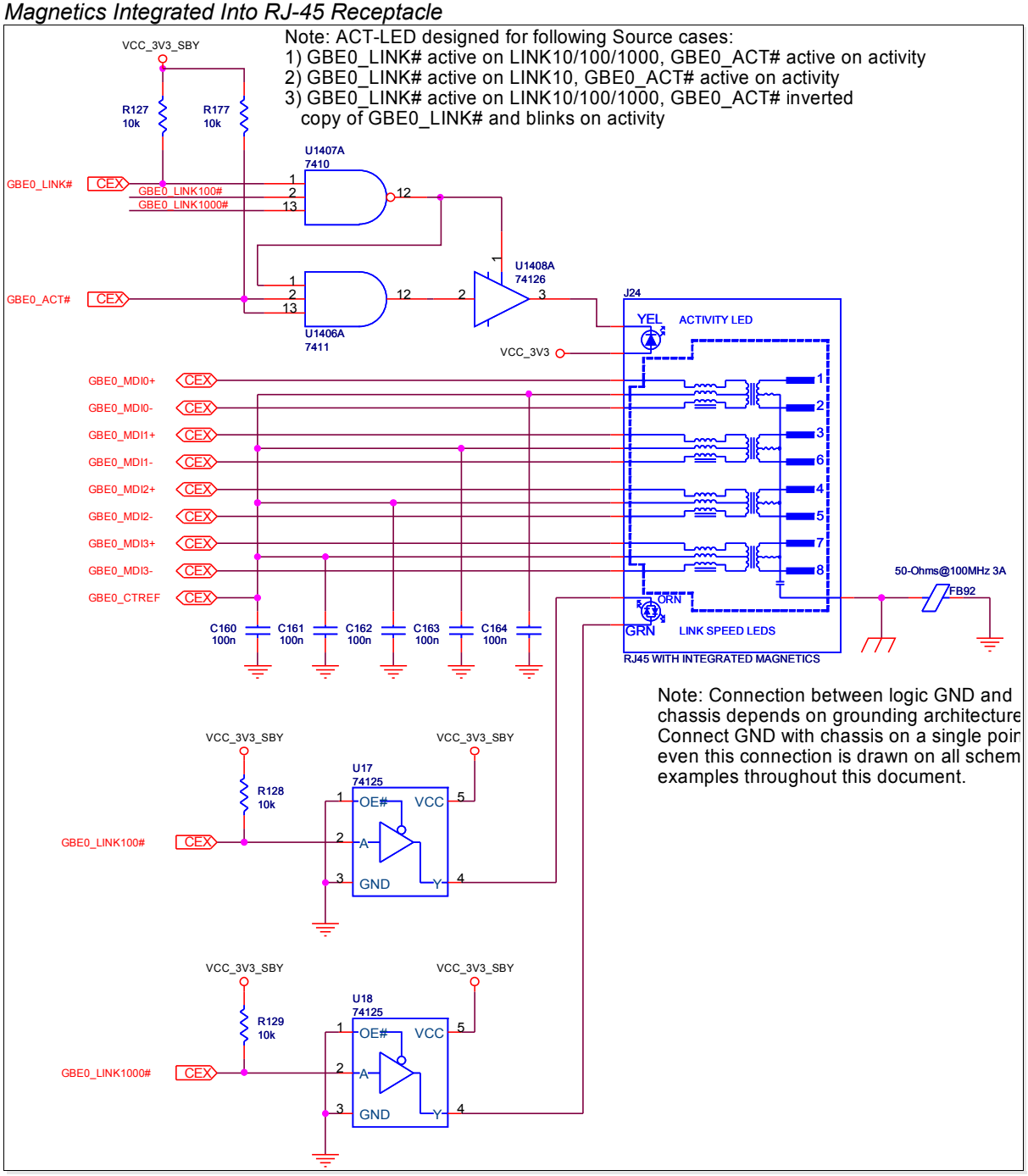
As there are a large number of Ethernet PHY components and coupling transformers on the market, it is strongly recommended that the Carrier Board vendor document the transformer used in this interface circuit, in order to facilitate interoperability analysis between Modules and carriers. It is also recommended that the COM Express Module vendor identify the specific PHY component used in the LAN 0 interface on the Module.

If the Carrier Board vendor chooses to support 4-wire 10/100BaseTX PHY circuits on the COM Express Module, the vendor should define the modifications required to the Carrier Board to support the 10/100BaseTX PHY. In general, it is recommended that the Carrier Board provide a method of changing the A and B pair transformer secondary center tap reference that does not require physically adding or removing components from the Carrier Board, in order to simplify Carrier Board reconfiguration work for different COM Express Modules.

2.6.2. Reference Schematics

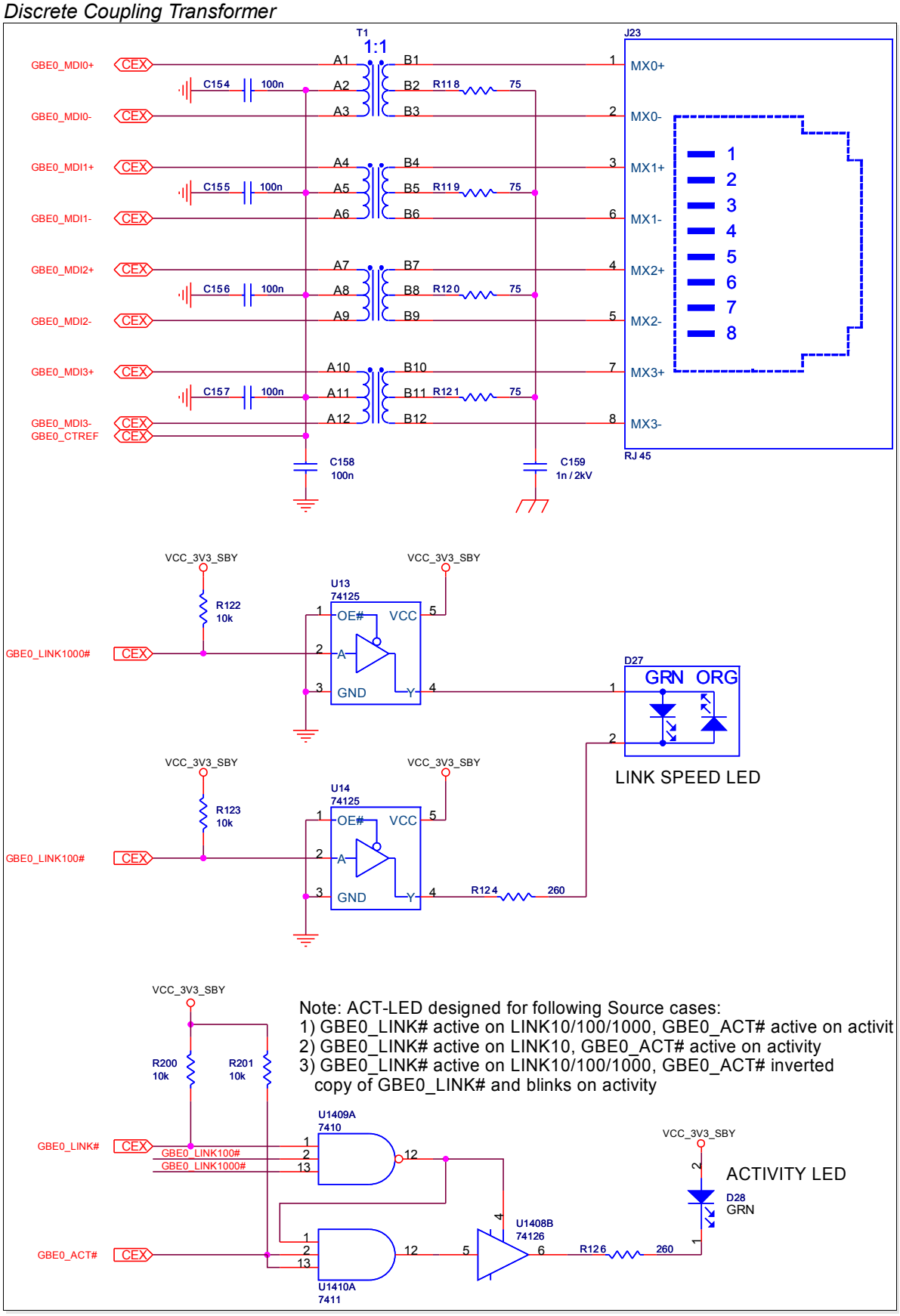
2.6.2.1. Magnetics Integrated Into RJ-45 Receptacle

Figure 18: Magnetics Integrated Into RJ-45 Receptacle



2.6.2.2. Discrete Coupling Transformer

Figure 19: Discrete Coupling Transformer



2.6.3. Routing Considerations

The 8-wire PHY / MDI circuit is required to meet a specific waveform template and associated signal integrity requirements defined in the IEEE 802.3-2005 specification. In order to meet these requirements, the routing rules in Section 6.4.5. 'LAN Trace Routing Guidelines' on page 136 should be observed on the Carrier Board.

The four status signals driven by the COM Express Module to the Carrier Board are low frequency signals that do not have any signal integrity or trace routing requirements beyond generally accepted design practices for such signals.

2.6.3.1. Reference Ground Isolation and Coupling

The Carrier Board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier's digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the Carrier Board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

2.7. USB Ports

A COM Express Module must support a minimum of 4 USB Ports and can support up to 8 USB Ports. All of the USB Ports must be USB2.0 compliant. There are 4 over-current signals shared by the 8 USB Ports . A Carrier must current limit the USB power source to minimize disruption of the Carrier in the event that a short or over-current condition exists on one of the USB Ports. A Module must fill the USB Ports starting at Port 0. Although USB signals use differential signaling, the USB specification also encodes single ended state information in the differential pair, making EMI filtering somewhat challenging. Ports that are internal to the Carrier do not need EMI filters. A USB Port can be powered from the Carrier Main Power or from the Carrier Suspend Power. Main Power is used for USB devices that are accessed when the system is powered on. Suspend Power (VCC_5V_SBY) is used for devices that need to be powered when the Module is in Sleep-State S5. This would typically be for USB devices that support Wake-on-USB. The amount of current available on VCC_5V_SBY is limited so it should be used sparingly.

2.7.1. Signal Definitions

All eight USB Ports appear on the COM Express A-B connector as shown in Table 13 below.

2.7.1.1. USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# unconnected.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB over-current protection and therefore can be used as a replacement for power distribution switches.

Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

2.7.1.2. Powering USB devices during S5

The power distribution switches and the ESD protection shown in the schematics can be powered from Main Power or Suspend Power (VCC_5V_SBY). Ports powered by Suspend Power are powered during the S3 and S5 system states. This provides the ability for the COM Express Module to generate system wake-up events over the USB interface.

Table 13: USB Signal Description

Signal	Pin #	Description	I/O	Comment
USB0+	A46	USB Port 0, data + or D+	I/O USB	mandatory
USB0-	A45	USB Port 0, data - or D-	I/O USB	mandatory
USB1+	B46	USB Port 1, data + or D+	I/O USB	mandatory
USB1-	B45	USB Port 1, data - or D-	I/O USB	mandatory
USB2+	A43	USB Port 2, data + or D+	I/O USB	mandatory
USB2-	A42	USB Port 2, data - or D-	I/O USB	mandatory
USB3+	B43	USB Port 3, data + or D+	I/O USB	mandatory
USB3-	B42	USB Port 3, data - or D-	I/O USB	mandatory
USB4+	A40	USB Port 4, data + or D+	I/O USB	optional
USB4-	A39	USB Port 4, data - or D-	I/O USB	optional
USB5+	B40	USB Port 5, data + or D+	I/O USB	optional
USB5-	B39	USB Port 5, data - or D-	I/O USB	optional
USB6+	A37	USB Port 6, data + or D+	I/O USB	optional
USB6-	A36	USB Port 6, data - or D-	I/O USB	optional
USB7+	B37	USB Port 7, data + or D+	I/O USB	optional
USB7-	B36	USB Port 7, data - or D-	I/O USB	optional
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1.	I 3.3V CMOS	optional
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3.	I 3.3VCMOS	optional
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5.	I 3.3V CMOS	optional
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7.	I 3.3V CMOS	optional

2.7.1.3. USB connector

Figure 20: USB Connector

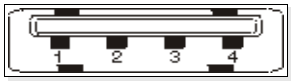


Table 14: USB Connector Signal Description

Signal	Pin	Description	I/O	Comment
VCC	1	+5V Power Supply	P 5V	Must be current-limited for external devices
-DATA	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
+DATA	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
GND	4	Ground	P	

2.7.2. Reference Schematics

The following notes apply to Figure 21 below.

J1 and J2 incorporate two USB Type A receptacles. J1, in addition, includes an RJ-45 (Foxconn UB11123-J51, Pulse JW0A1P0R-E).

The reference design uses an over-current detection and protection device. Two examples are the Texas Instruments TPS2042AD and the Micrel MIC2026 dual channel power distribution switch. The second example includes a discrete implementation.

The first schematic is powered from VCC_5V_SBY Suspend power and can provide Wake on LAN support. The second schematic is powered using 5V.

Power to the USB Port is filtered using a ferrite (90 Ω @100MHz, 3000mA) to minimize emissions. The ferrite should be placed adjacent to the USB Port connector pins.

USB_0_1_OC# and USB_2_3_OC# are over-current signals that are inputs to COM Express Module. Each signal is driven low upon detection of overload, short-circuit or thermal trip, which causes the affected USB Port power to turn off. Do not attach pull-ups to the OC signals on the COM Express Carrier Board; this is done on the COM Express Module.

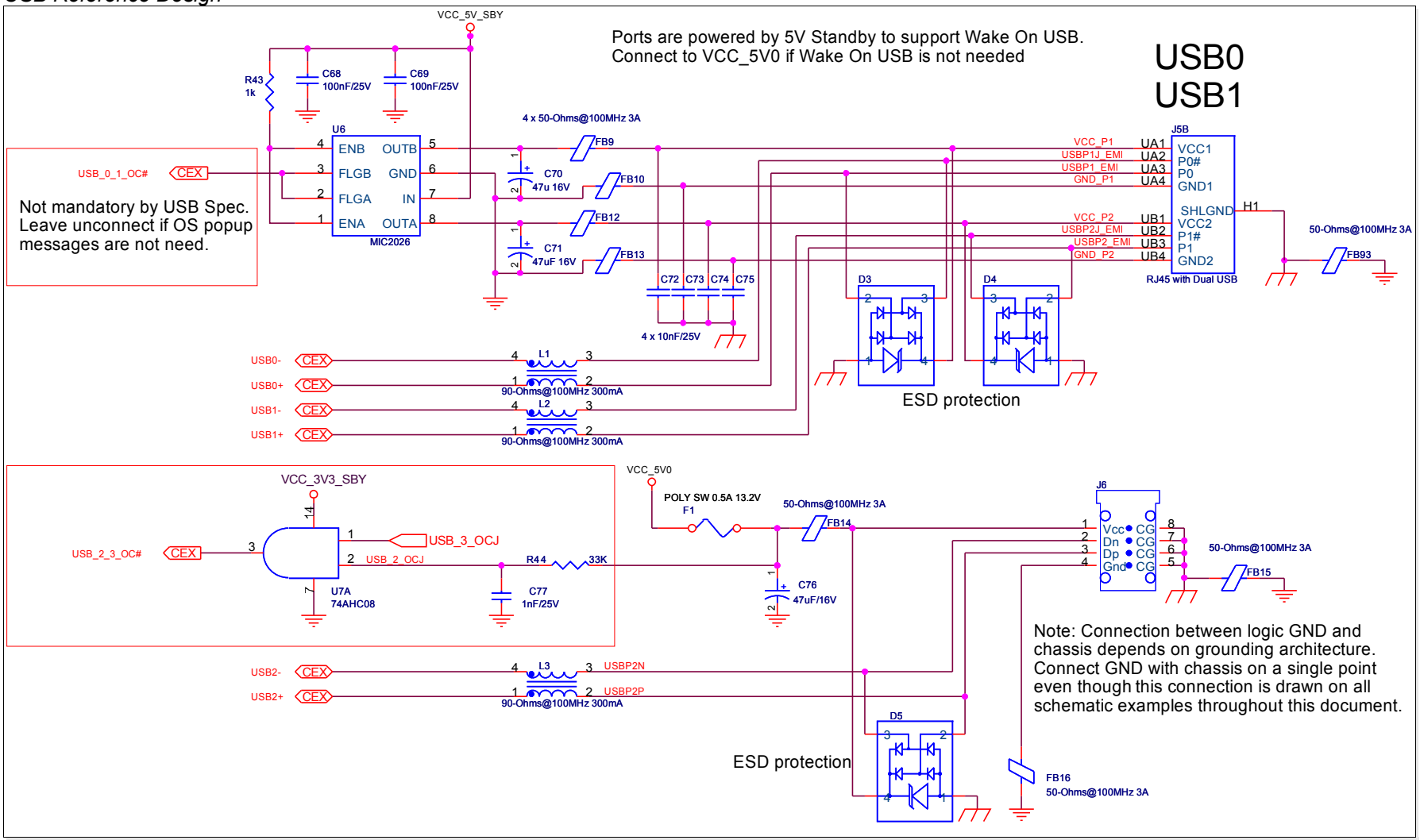
The OC# signal is asserted until the over-current or over-temperature condition is resolved.

USB0+/- through USB2+/- from the COM Express Module are routed through a common mode choke to reduce radiated cable emissions. The part shown is a Coilcraft 0805USB-901MLC; this device has a common mode impedance of approximately 90 Ω at 100MHz. The common-mode choke should be placed close to the USB connector.

ESD protection diodes D1 and D2 provide overvoltage protection caused by ESD and electrical fast transients . Low capacitance diodes and transient voltage suppression diodes should be placed near the USB connector. The example design uses a SR05 RailClamp surge diode array DATVSSR05 from Semtech (http://semtech.com).

The example designs show a ferrite connecting Chassis Ground and Logic Ground at the USB connector. Many USB devices connect Chassis and Logic grounds together. To minimize the current in this path a ferrite or capacitor connecting Chassis Ground to Logic Ground should be placed close to the USB connector.

Figure 21: USB Reference Design



2.7.3. Routing Considerations

Route USB signals as differential pairs, with a 90-Ω differential impedance and a 45-Ω, single-ended impedance. Ideally, a USB pair is routed on a single layer adjacent to a ground plane.

USB pairs should not cross plane splits. Keep layer transitions to a minimum. Reference USB pairs to a power plane if necessary. The power plane should be well-bypassed. Section 6.4.2. 'USB Trace Routing Guidelines' on page 133 summarizes USB routing rules.

2.7.3.1. EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design. In the USB reference schematics Figure 21 above, this is implemented by using 'SR05 RailClamp®' surge rated diode arrays from Semtech (http://semtech.com).

2.8. SATA

Support for up to four SATA ports is defined on the COM Express A-B connector. Support for a minimum of two ports is required for all Module Types. The COM Express Specification allows for both SATA-150 and SATA-300 implementations. Constraints for SATA-300 implementations are more severe than those for SATA-150. The COM Express Specification addresses both in the section on insertion losses.

SATA devices can be internal to the system or external. The eSATA specification defines the connector used for external SATA devices. The eSATA interface must be designed to prevent damage from ESD, comply with EMI limits, and withstand more insertion/removals cycles than standard SATA. A specific eSATA connector was designed to meet these needs. The eSATA connector does not have the “L” shaped key, and because of this, SATA and eSATA cables cannot be interchanged.

2.8.1. Signal Definitions

Table 15: SATA Signal Description

Signal	Pin	Description	I/O	Comment
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0 Receive input differential pair.	I SATA	
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0 Transmit output differential pair.	O SATA	
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1 Receive input differential pair.	I SATA	
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1 Transmit output differential pair.	O SATA	
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2 Receive input differential pair.	I SATA	
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2 Transmit output differential pair.	O SATA	
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3 Receive input differential pair.	I SATA	
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3 Transmit output differential pair.	O SATA	
SATA_ACT#	A28	Serial ATA activity LED. Open collector output pin driven during SATA command activity.	O 3.3V CMOS OC	Able to drive 10 mA

Table 16: Serial ATA Connector Pinout

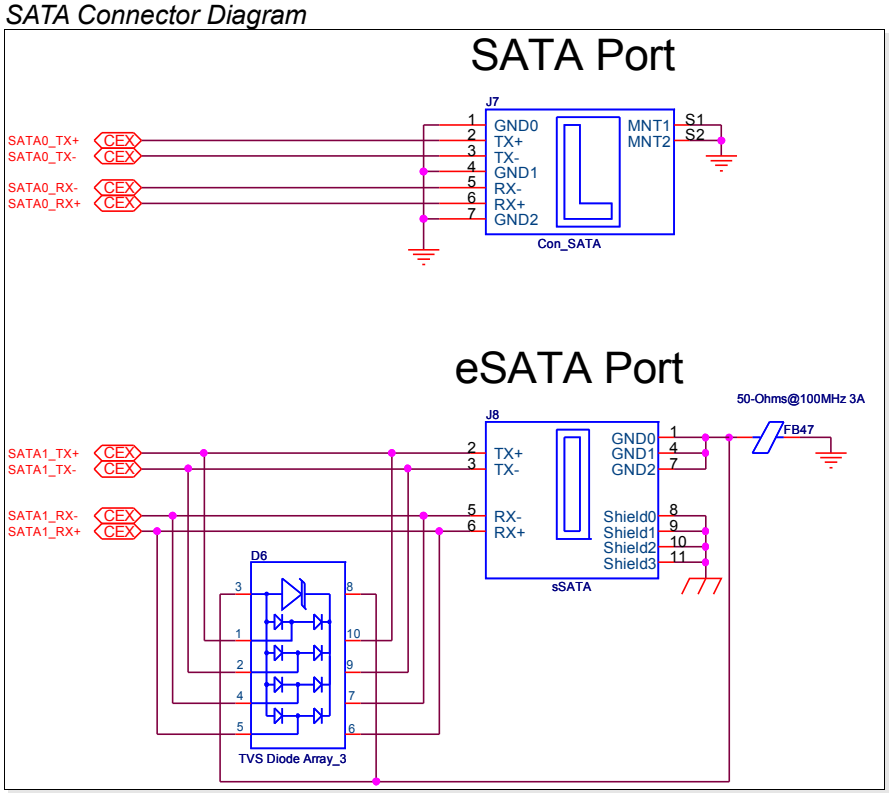
Pin	Signal	Description
1	GND	Ground
2	TX+	Transmitter differential pair positive signal
3	TX-	Transmitter differential pair negative signal
4	GND	Ground
5	RX-	Receiver differential pair negative signal
6	RX+	Receiver differential pair positive signal
7	GND	Ground

Table 17: Serial ATA Power Connector Pinout

Pins	Signal	Description
1,2,3	+3.3V	3.3V power supply
4,5,6	GND	Ground
7,8,9	+5V	5V power supply
10,11,12	GND	Ground
13,14,15	+12V	12V power supply

2.8.2. Reference Schematic

Figure 22: SATA Connector Diagram



The following notes apply to Figure 22 above.

The Module provides a single LED signal SATA_ACT# that can be used to indicate SATA drive activity.

The SATA connector shown is a Molex 67491-0019, a 1.27mm-pitch 7-pin high-speed vertical plug.

The example design contains the SATA data and ground signals only. Power is provided through a separate connector from the system power supply. Alternate 22-pin connector types are available that deliver power and data to the SATA drive. This may be over a combined power/data cable or in a direct configuration in which the SATA drive mates directly to the 22-pin plug on the Carrier Board. Please refer to the SATA specification (Appendix G) for pin-out information.

ESD clamp diodes such as Semtech Rclamp0524 are shown in the eSATA schematic. This device contains low capacitance clamp diodes. The schematic shows two connections on each SATA signal to the clamp diodes. The second connection is actually a no-connect on the package and allows for straight-through routing for the SATA differential pairs.

Nets SATA0_TX+/- through SATA1_TX +/- are sourced from the COM Express Module SATA TX pins.

Nets SATA0_RX+/- through SATA1_RX +/- are sourced from SATA disks and are routed to the COM Express Module SATA RX pins.

Coupling capacitors are not needed on Carrier Board SATA lines. They are present on the COM Express Module.

2.8.3. Routing Considerations

Route SATA signals as differential pairs, with a 100 Ω differential impedance and a 55 Ω, single-ended impedance. Ideally, a SATA pair is routed on a single layer adjacent to a ground plane. SATA pairs should not cross plane splits. Keep layer transitions to a minimum. Reference SATA pairs to a power plane if necessary. The power plane should be quiet and well bypassed. SATA-150 routing rules are also summarized in Section 6.4.6. 'Serial ATA Trace Routing Guidelines' on page 137.

2.9. LVDS

2.9.1. Signal Definitions

The COM Express Specification provides an optional LVDS interface on the COM Express A-B connector. Module pins for two LVDS channels are defined and designated as LVDS_A and LVDS_B.

Systems use a single-channel LVDS for most displays. Dual LVDS channels are used for very high-bandwidth displays. Single-channel LVDS means that one complete RGB pixel is transmitted per display input clock (also known as the shift clock - see Table 18 'LVDS Signal Descriptions' below for a summary of LVDS terms). Dual-channel LVDS means that two complete RGB pixels are transmitted per display input clock. The two pixels are adjacent along a display line. Dual-channel LVDS does not mean that two LVDS displays can be driven.

Each COM Express LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. COM Express Modules and Module chipsets may not use all pairs. For example, with 18-bit TFT displays, only three of the four data pairs on the LVDS_A channel are used, along with the LVDS_A clock. The LVDS_B lines are not used. The manner in which RGB data is packed onto the LVDS pairs (including packing order and color depth) is not specified by the COM Express Specification. This may be Module-dependent. Further mapping details are given in Section 2.9.1.6. 'LVDS Display Color Mapping Tables' below.

There are five single-ended signals included to support the LVDS interface: two lines are used for an I2C interface that may be used to support EDID or other panel information and identification schemes. Additionally, there are an LVDS power enable (LVDS_VDD_EN) and backlight control and enable lines (LVDS_BKLT_CTRL and LVDS_BKLT_EN).

Table 18: LVDS Signal Descriptions

Signal	Pin	Description	I/O	Comment
LVDS_A0+ LVDS_A0-	A71 A72	LVDS channel A differential signal pair 0	O LVDS	
LVDS_A1+ LVDS_A1-	A73 A74	LVDS channel A differential signal pair 1	O LVDS	
LVDS_A2+ LVDS_A2-	A75 A76	LVDS channel A differential signal pair 2	O LVDS	
LVDS_A3+ LVDS_A3-	A78 A79	LVDS channel A differential signal pair 3	O LVDS	
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS channel A differential clock pair	O LVDS	
LVDS_B0+ LVDS_B0-	B71 B72	LVDS channel B differential signal pair 0	O LVDS	
LVDS_B1+ LVDS_B1-	B73 B74	LVDS channel B differential signal pair 1	O LVDS	
LVDS_B2+ LVDS_B2-	B75 B76	LVDS channel B differential signal pair 2	O LVDS	
LVDS_B3+ LVDS_B3-	B77 B78	LVDS channel B differential signal pair 3	O LVDS	
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS channel B differential clock pair	O LVDS	
LVDS_VDD_EN	A77	LVDS flat panel power enable.	O 3.3V, CMOS	
LVDS_BKLT_EN	B79	LVDS flat panel backlight enable high active signal	O 3.3V, CMOS	
LVDS_BKLT_CTRL	B83	LVDS flat panel backlight brightness control	O 3.3V, CMOS	
LVDS_I2C_CK	A83	DDC I2C clock signal used for flat panel detection and control.	O 3.3V, CMOS	
LVDS_I2C_DAT	A84	DDC I2C data signal used for flat panel detection and control.	I/O 3.3V, OD CMOS	

2.9.1.1. Connector and Cable Considerations

When implementing LVDS signal pairs on a single-ended Carrier Board connector, the signals of a pair should be arranged so that the positive and negative signals are side by side. The trace lengths of the LVDS signal pairs between the COM Express Module and the connector on the Carrier Board should be the same as possible. Additionally, one or more ground traces/pins must be placed between the LVDS pairs.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver.

Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Ribbon cables are a cost effective and easy solution. Even though they are not well suited for high-speed differential signaling they do work fine for very short runs. Most cables will work effectively for cable distances of <0.5m.

The cables and connectors that are to be utilized should have a differential impedance of 100Ω ±15%. They should not introduce major impedance discontinuities that cause signal reflections.

For more informations about this subject, refer to the 'LVDS Owners Manual Section 6' available from National Semiconductor (http://www.national.com).

2.9.1.2. Display Timing Configuration

The graphic controller needs to be configured to match the timing parameters of the attached flat panel display. To properly configure the controller, there needs to be some method to determine the display parameters. Different Module vendors provide differing ways to access display timing parameters. Some vendors store the data in non-volatile memory with the BIOS setup screen as the method for entering the data, other vendors might use a Module or Carrier based EEPROM. Some vendors might hard code the information into the BIOS, and other vendors might support panel located timing via the signals LVDS_I2C_CK and LVDS_I2C_DAT with an EEPROM strapped to 1010 000x. Regardless of the method used to store the panel timing parameters, the video BIOS will need to have the ability to access and decode the parameters. Given the number of variables it is recommended that Carrier designers contact Module suppliers to determine the recommend method to store and retrieve the display timing parameters.

The Video Electronics Standards Association (VESA) recently released DisplayID, a second generation display identification standard that replaces EDID and other proprietary methods for storing flat panel timing data. DisplayID defines a data structure which contains information such as display model, identification information, colorimetry, feature support, and supported timings and formats. The DisplayID data allows the video controller to be configured for optimal support for the attached display without user intervention. The basic data structure is a variable length block up to 256 bytes with additional 256 byte extensions as required. The DisplayID data is typically stored in a serial EPROM connected to the LVDS_I2C bus. The EPROM can reside on the display or Carrier. DisplayID is not backwards compatible with EDID. Contact VESA (www.vesa.org) for more information.

2.9.1.3. Backlight Control

Backlight inverters are either voltage, PWM or resistor controlled. The COM Express specification provides two methods for controlling the brightness. One method is to use the backlight control and enable signals from the CPU chipset. These signals are brought on COM Express LVDS_BKLT_EN and LVDS_BKLT_CTRL. LVDS_BKLT_CTRL is a Pulse Width Modulated (PWM) output that can be connected to display inverters that accept a PWM input. The second method it to use the LVDS I2C bus to control an I2C DAC. The output of the DAC can be used to support voltage controlled inverters. The DAC can be used driving the backlight voltage control input pin of the inverter. The reference design shown in Figure 23 on page 66 below supports this. A header is used to allow the user to configure the type of backlight inverter signal used. In the example a DAC from Maxim is used (MAX5362 http://www.maxim.com).

2.9.1.4. Color Mapping and Terms

FPD-Link and Open LDI Color Mapping

An LVDS stream consists of frames that pack seven data bits per LVDS frame. Details can be found in the tables below. The LVDS clock is one seventh of the source-data clock. The order in which panel data bits are packed into the LVDS stream is referred to as the LVDS color-mapping. There are two LVDS color-mappings in common use: FPD-Link and Open LDI. Open LDI is the newer standard.

The FPD-Link and Open LDI standards are the same for panels with color depths of 18 bits (6 Red, 6 Green, 6 Blue) or less. The 18 bits of color data and 3 bits of control data, or 21 bits total, are packed into 3 LVDS data streams. The LVDS clock is carried on a separate channel for a total of 4 LVDS pairs – 3 data pairs and a clock pair.

For 24-bit color depths, a 4th LVDS data pair is required (for a total of 5 LVDS pairs – 4 data and 1 clock). FPD-Link and Open LDI differ in this case. FPD-Link keeps the least significant color bits on the original 3 LVDS data pairs and adds the most significant color bits (the dominant or “most important” bits) to the 4th channel. Six bits are added: 2 Red, 2 Green, and 2 Blue (the seventh available bit slot in the 4th LVDS stream is not used).

A 24-bit, Open LDI implementation shifts the color bits on the original 3 LVDS data pairs up by two, such that the most significant color bits for both 18- and 24-bit panels occupy the same LVDS slots. For example, the most significant Red color bit is R5 for 18-bit panels and R7 for 24-bit panels. The 18-bit R5 and the 24-bit R7 occupy the same LVDS bit slot in Open LDI. The 4th LVDS data stream in Open LDI carries the least significant bits of a 24-bit panel – R0, R1, G0, G1, B0, and B1.

The advantage of Open LDI is that it provides an easier upgrade and downgrade path than FPD-Link does. An 18-bit panel can be used with an Open LDI 24-bit data stream by simply connecting the 1st three LVDS data pairs to the panel, and leaving the 4th LVDS data pair unused. This does not work with FPD-Link because the mapping for the 24-bit case is not compatible with the 18-bit case – the most significant data bits are on the 4th LVDS data stream.

If you design LVDS deserializers, work around the Module color-mapping by picking off the deserializer outputs in the order needed. If you use a flat panel with an integrated LVDS receiver, it is important that the displays color-mapping matches the Module’s color-mapping.

Table 19: LVDS Display Terms and Definitions

Term	Definition
Color-Mapping	Color-mapping refers to the order in which display color bits and control bits are placed into the serial LVDS stream. Each LVDS data frame can accept seven bits. The way in which the bits are serialized into the stream is arbitrary, as long as they are de-serialized in a corresponding way. Two main color-mapping schemes are FPD-Link and Open LDI. They are the same for 18-bit panels but differ for 24-bit panels.
DE	Display Enable – a control signal that asserts during an active display line.
Dual Channel	In a dual-channel bit stream, two complete RGB pixels are transmitted with each shift clock. The shift clock is one half the pixel frequency in this case. Dual channel LVDS streams are either 8 differential pairs (6 data pairs, 2 clock pairs, for dual 18 bit streams) or 10 differential pairs (8 data pairs, 2 clock pairs, for dual 24-bit streams).
Even Pixel	A pixel from an even column number, counting from 1. For example, on an 800x600 display, the even pixels along a row are in columns 2,4 … 800. The odd pixels are in columns 1,3,5 … 799.
FPD-Link	Flat Panel Display Link – an LVDS color-mapping scheme popularized by National Semiconductor. FPD Link color-mapping is the same as open LDI color-mapping for 18-bit displays but is different for 24-bit displays. FPD color-mapping puts the most significant bits of a 24-bit display onto the 4th LVDS channel.
HSYNC	Horizontal Sync – a control signal that occurs once per horizontal display line.
LCLK	LVDS clock – the low voltage differential clock that accompanies the serialized LVDS data stream. For a single-channel LVDS stream, the LVDS clock is 1/7th the pixel clock, which means there is one LVDS clock period for every 7 pixel clock periods. For a dual-channel LVDS data stream, the LVDS clock is 1/14th the pixel clock, which means there is one LVDS clock period for every 14-pixel clock periods.
Odd Pixel	A pixel from an odd column number, counting from 1. For example, on an 800x600 display, the odd pixels along a row are in columns 1,3,5, … 799. The even pixels are in columns 2,4 …800.
Open LDI	Open LVDS Display Interface – a formalization by National Semiconductor of de facto LVDS standards. See Appendix G for a reference to the standard. Open LDI color-mapping is the same as FPD-Link color-mapping for 18-bit displays, but is different for 24-bit displays. Open LDI color-mapping puts the least significant bits of a 24-bit display onto the 4th LVDS channel. Doing so means that an 18-bit display can operate on a 24-bit Open LDI link by using the first 3 LVDS data channels.
PCLK	Pixel clock – the clock associated with a single display pixel. For example, on a 640x480 display, there are 640 pixel clocks during the active display line period (and additional pixel clocks during the blanking periods). For a single-channel TFT display, the pixel clock is the same as the shift clock. For a dual-channel TFT display, the pixel clock is twice the frequency of the shift clock.
SCLK	Shift clock – the clock that shifts either a single pixel or a group of pixels into the display, depending on the display type. For a single-channel TFT display, the shift clock is the same as the pixel clock. For a dual-channel TFT display, the shift clock period is twice the pixel clock. For some display types, such as passive STN displays, the shift clock may be four- or eight-pixel clocks.
Single Channel	In a single-channel bit stream, a single RGB pixel is transmitted with each shift clock. The shift clock and the pixel clock are the same in this case. Single-channel LVDS streams are either 4 differential pairs (3 data pairs, 1 clock pair, for a single 18 bit stream) or 5 differential pairs (4 data pairs, 1 clock pair, for a single 24-bit stream).
Transmit Bit Order	The order, in time, in which bits are placed into the seven bit slots per LVDS frame. Bit 1 is earlier in time than bit 2, etc.
Unbalanced	Unbalanced means that the LVDS serializing hardware does not insert or manipulate bits to achieve a DC balance – i.e. an equal number of 0 and 1 bits, when averaged over multiple frames.
VSYNC	Vertical Sync – a control signal that occurs once per display frame.
Xmit Bit Order	See Transmit Bit Order.

2.9.1.5. Note on Industry Terms

Some terms in this document that describe LVDS displays may vary from other documents (such as display data sheets from vendors, IC data sheets for graphics controllers and LVDS transmitters and receivers, the Open LDI specification, and COM Express Module documentation).

Examples of terms that may vary include:

For dual-channel displays, terms are needed to describe the adjacent pixels.

Various documents will reference for the same pair of pixels:

Odd and Even pixels (column count starts at 1)

Even and Odd pixels (column count starts at 0)

R10 and R20 for adjacent least significant Red bits

R00 and R10 for adjacent least significant Red bits

Terms used to describe the clocks vary:

The Open LDI specification uses the term “pixel clock” differently from most other documents. In the Open LDI specification, the “pixel clock” period is seven pixel periods long. Most other documents refer to this concept as the “LVDS clock.”

Transmit Bit Order

In this document, the seven bits in an LVDS frame are numbered 1 – 7, with Bit 1 being placed into the stream before Bit 2.

Display terms used in this document are defined in Table 19 above.

2.9.1.6. LVDS Display Color Mapping Tables

LVDS display color-mappings for single- and dual-channel displays are shown in Table 20 and Table 21 below.

For single-channel displays, COM Express Module LVDS B pairs are not used and may be left open. For single-channel, 18-bit displays, the LVDS_A3± channel is not used and may be left open.

For 18-bit, single-channel and 36-bit, dual-channel displays, the FPD-Link and Open LDI color-mappings are the same. For 24-bit, single-channel and 48-bit, dual-channel displays, mappings differ and care must be taken that the Module and display LVDS color-mappings agree.

Table 20: LVDS Display: Single Channel, Unbalanced Color-Mapping

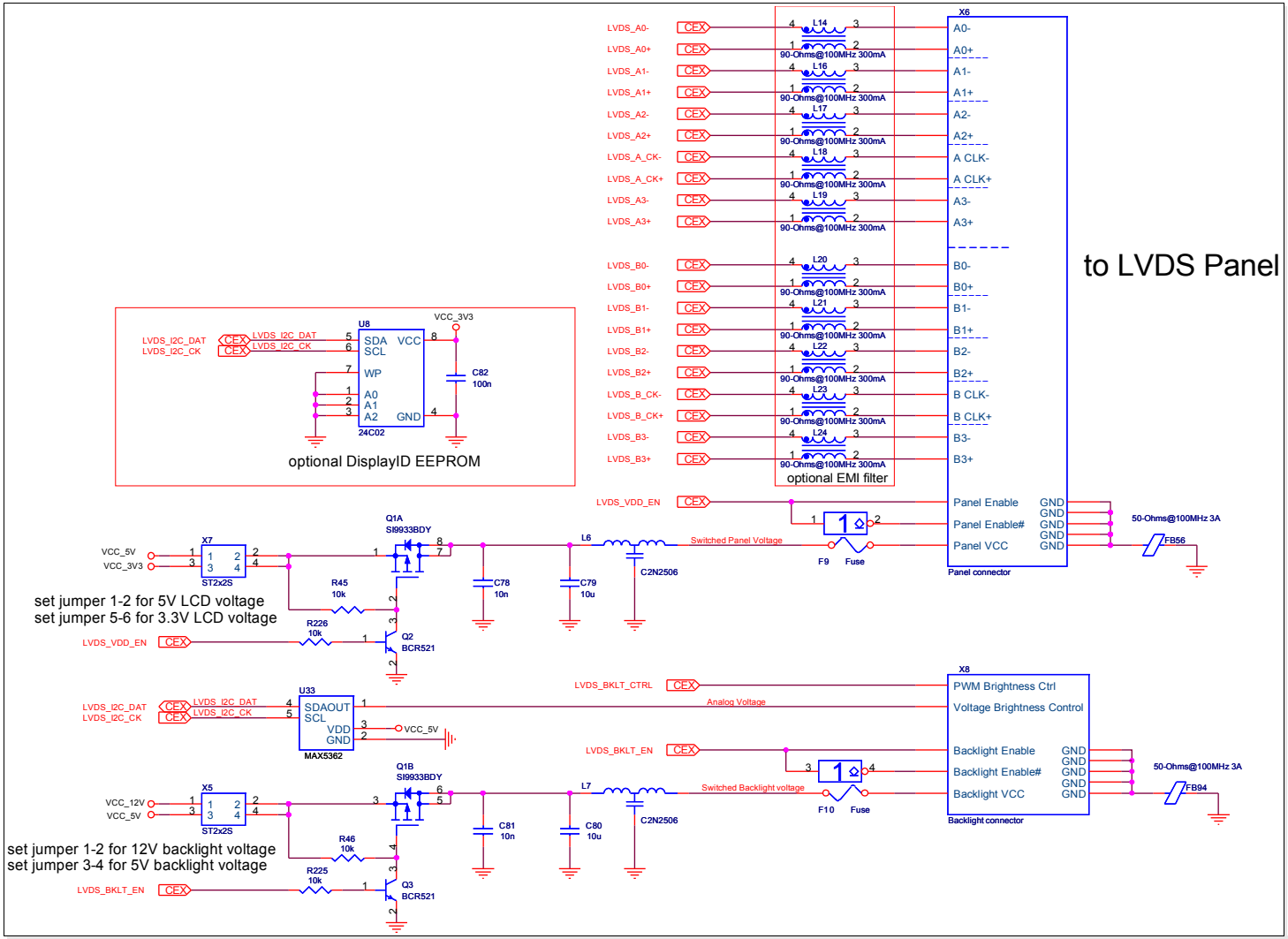
	Xmit Bit Order	LVDS Clock	Open LDI 18 bit Single Ch	Open LDI 24 bit Single Ch	FPD Link 18 bit Single Ch	FPD Link 24 bit Single Ch
LVDS_A0±	1	1	G0	G2	G0	G0
	2	1	R5	R7	R5	R5
	3	0	R4	R6	R4	R4
	4	0	R3	R5	R3	R3
	5	0	R2	R4	R2	R2
	6	1	R1	R3	R1	R1
	7	1	R0	R2	R0	R0
LVDS_A1±	1	1	B1	B3	B1	B1
	2	1	B0	B2	B0	B0
	3	0	G5	G7	G5	G5
	4	0	G4	G6	G4	G4
	5	0	G3	G5	G3	G3
	6	1	G2	G4	G2	G2
	7	1	G1	G3	G1	G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	B5	B7	B5	B5
	5	0	B4	B6	B4	B4
	6	1	B3	B5	B3	B3
	7	1	B2	B4	B2	B2
LVDS_A3±	1	1				
	2	1		B1		B7
	3	0		B0		B6
	4	0		G1		G7
	5	0		G0		G6
	6	1		R1		R7
	7	1		R0		R6
LVDS_A_CK±			LCLK = PCLK / 7 SCLK = PCLK	LCLK= PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK	LCLK = PCLK / 7 SCLK = PCLK

Table 21: LVDS Display: Dual Channel, Unbalanced Color-Mapping

	Xmit Bit Order	LVDS Clock	Open LDI 18 bit (36 bit) Dual Ch	Open LDI 24 bit (48 bit) Dual Ch	FPD Link 18 bit (36 bit) Dual Ch	FPD Link 24 bit (48 bit) Dual Ch
LVDS_A0±	1	1	Odd Pixel G0	Odd Pixel G2	Odd Pixel G0	Odd Pixel G0
	2	1	Odd Pixel R5	Odd Pixel R7	Odd Pixel R5	Odd Pixel R5
	3	0	Odd Pixel R4	Odd Pixel R6	Odd Pixel R4	Odd Pixel R4
	4	0	Odd Pixel R3	Odd Pixel R5	Odd Pixel R3	Odd Pixel R3
	5	0	Odd Pixel R2	Odd Pixel R4	Odd Pixel R2	Odd Pixel R2
	6	1	Odd Pixel R1	Odd Pixel R3	Odd Pixel R1	Odd Pixel R1
	7	1	Odd Pixel R0	Odd Pixel R2	Odd Pixel R0	Odd Pixel R0
LVDS_A1±	1	1	Odd Pixel B1	Odd Pixel B3	Odd Pixel B1	Odd Pixel B1
	2	1	Odd Pixel B0	Odd Pixel B2	Odd Pixel B0	Odd Pixel B0
	3	0	Odd Pixel G5	Odd Pixel G7	Odd Pixel G5	Odd Pixel G5
	4	0	Odd Pixel G4	Odd Pixel G6	Odd Pixel G4	Odd Pixel G4
	5	0	Odd Pixel G3	Odd Pixel G5	Odd Pixel G3	Odd Pixel G3
	6	1	Odd Pixel G2	Odd Pixel G4	Odd Pixel G2	Odd Pixel G2
	7	1	Odd Pixel G1	Odd Pixel G3	Odd Pixel G1	Odd Pixel G1
LVDS_A2±	1	1	DE	DE	DE	DE
	2	1	VSYNC	VSYNC	VSYNC	VSYNC
	3	0	HSYNC	HSYNC	HSYNC	HSYNC
	4	0	Odd Pixel B5	Odd Pixel B7	Odd Pixel B5	Odd Pixel B5
	5	0	Odd Pixel B4	Odd Pixel B6	Odd Pixel B4	Odd Pixel B4
	6	1	Odd Pixel B3	Odd Pixel B5	Odd Pixel B3	Odd Pixel B3
	7	1	Odd Pixel B2	Odd Pixel B4	Odd Pixel B2	Odd Pixel B2
LVDS_A3±	1	1				
	2	1		Odd Pixel B1		Odd Pixel B7
	3	0		Odd Pixel B0		Odd Pixel B6
	4	0		Odd Pixel G1		Odd Pixel G7
	5	0		Odd Pixel G0		Odd Pixel G6
	6	1		Odd Pixel R1		Odd Pixel R7
	7	1		Odd Pixel R0		Odd Pixel R6
LVDS_A_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2
LVDS_B0±	1	1	Even Pixel G0	Even Pixel G2	Even Pixel G0	Even Pixel G0
	2	1	Even Pixel R5	Even Pixel R7	Even Pixel R5	Even Pixel R5
	3	0	Even Pixel R4	Even Pixel R6	Even Pixel R4	Even Pixel R4
	4	0	Even Pixel R3	Even Pixel R5	Even Pixel R3	Even Pixel R3
	5	0	Even Pixel R2	Even Pixel R4	Even Pixel R2	Even Pixel R2
	6	1	Even Pixel R1	Even Pixel R3	Even Pixel R1	Even Pixel R1
	7	1	Even Pixel R0	Even Pixel R2	Even Pixel R0	Even Pixel R0
LVDS_B1±	1	1	Even Pixel B1	Even Pixel B3	Even Pixel B1	Even Pixel B1
	2	1	Even Pixel B0	Even Pixel B2	Even Pixel B0	Even Pixel B0
	3	0	Even Pixel G5	Even Pixel G7	Even Pixel G5	Even Pixel G5
	4	0	Even Pixel G4	Even Pixel G6	Even Pixel G4	Even Pixel G4
	5	0	Even Pixel G3	Even Pixel G5	Even Pixel G3	Even Pixel G3
	6	1	Even Pixel G2	Even Pixel G4	Even Pixel G2	Even Pixel G2
	7	1	Even Pixel G1	Even Pixel G3	Even Pixel G1	Even Pixel G1
LVDS_B2±	1	1				
	2	1				
	3	0				
	4	0	Even Pixel B5	Even Pixel B7	Even Pixel B5	Even Pixel B5
	5	0	Even Pixel B4	Even Pixel B6	Even Pixel B4	Even Pixel B4
	6	1	Even Pixel B3	Even Pixel B5	Even Pixel B3	Even Pixel B3
	7	1	Even Pixel B2	Even Pixel B4	Even Pixel B2	Even Pixel B2
LVDS_B3±	1	1				
	2	1		Even Pixel B1		Even Pixel B7
	3	0		Even Pixel B0		Even Pixel B6
	4	0		Even Pixel G1		Even Pixel G7
	5	0		Even Pixel G0		Even Pixel G6
	6	1		Even Pixel R1		Even Pixel R7
	7	1		Even Pixel R0		Even Pixel R6
LVDS_B_CK±			LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2	LCLK= PCLK / 14 SCLK = PCLK / 2	LCLK = PCLK / 14 SCLK = PCLK / 2

2.9.2. Reference Schematics

Figure 23: LVDS Reference Schematic



2.9.3. Routing Considerations

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. Reference LVDS pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.

All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

LVDS routing rules are summarized in 6.4.7. 'LVDS Trace Routing Guidelines' on page 138 below.

2.10. IDE and CompactFlash (PATA)

2.10.1. Signal Definitions

Type 2 and 4 COM Express Modules provide a single channel IDE interface supporting two standard IDE hard drives or ATAPI devices with a maximum transfer rate of ATA100 (Ultra-DMA-100 with 100MB/s transfer rate). The corresponding signals can be found on the Module connector rows C and D.

Table 22: Parallel ATA Signal Descriptions

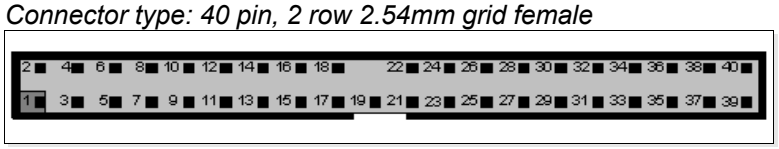
Signal	Pin	Description	I/O	IDE40	IDE44	CF
IDE_D0	D7	Bidirectional data to / from IDE device.	I/O 3.3V	17	17	21
IDE_D1	C10	Bidirectional data to / from IDE device.	I/O 3.3V	15	15	22
IDE_D2	C8	Bidirectional data to / from IDE device.	I/O 3.3V	13	13	23
IDE_D3	C4	Bidirectional data to / from IDE device.	I/O 3.3V	11	11	2
IDE_D4	D6	Bidirectional data to / from IDE device.	I/O 3.3V	9	9	3
IDE_D5	D2	Bidirectional data to / from IDE device.	I/O 3.3V	7	7	4
IDE_D6	C3	Bidirectional data to / from IDE device.	I/O 3.3V	5	5	5
IDE_D7	C2	Bidirectional data to / from IDE device.	I/O 3.3V	3	3	6
IDE_D8	C6	Bidirectional data to / from IDE device.	I/O 3.3V	4	4	47
IDE_D9	C7	Bidirectional data to / from IDE device.	I/O 3.3V	6	6	48
IDE_D10	D3	Bidirectional data to / from IDE device.	I/O 3.3V	8	8	49
IDE_D11	D4	Bidirectional data to / from IDE device.	I/O 3.3V	10	10	27
IDE_D12	D5	Bidirectional data to / from IDE device.	I/O 3.3V	12	12	28
IDE_D13	C9	Bidirectional data to / from IDE device.	I/O 3.3V	14	14	29
IDE_D14	C12	Bidirectional data to / from IDE device.	I/O 3.3V	16	16	30
IDE_D15	C5	Bidirectional data to / from IDE device.	I/O 3.3V	18	18	31
IDE_A[0:2]	D13-D15	Address lines to IDE device.	O 3.3V	35, 33, 36	35, 33, 36	20, 19, 18
IDE_IOW#	D9	I/O write line to IDE device.	O 3.3V	23	23	35
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V	25	25	34
IDE_REQ	D8	IDE device DMA request. It is asserted by the IDE device to request a data transfer.	I 3.3V	21	21	37
IDE_ACK#	D10	IDE device DMA acknowledge.	O 3.3V	29	29	44
IDE_CS1#	D16	IDE device chip select for 1F0h to 1FFh range.	O 3.3V	37	37	7
IDE_CS3#	D17	IDE device chip select for 3F0h to 3FFh range.	O 3.3V	38	38	32
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	I 3.3V	27	27	42
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V	1	1	41
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V	31	31	43
IDE_CBLID#	D77	Input from off-Module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 modes.	I 3.3V	34	34	46
DASP				39	39	45
GND				2, 19, 22, 24, 26, 30, 40	2, 19, 22, 24, 26, 30, 40, 43	17, 16, 15, 14, 12, 11, 10, 8, 12, 6, 9, 33, 25, 26 39 (master)

Signal	Pin	Description	I/O	IDE40	IDE44	CF
CSEL				28	28	39
N.C.				20, 32	20, 32, 44	24, 40, 51, 52, 53, 54, 55, 56 39 (slave)
VCC_5V					41, 42,	13, 18, 36

2.10.2. IDE 40-Pin Header (3.5 Inch Drives)

To interface standard 3.5-inch parallel ATA drives, a standard 2.54mm, two row, 40-pin connector in combination with a ribbon conductor cable is used. For slower drive speeds up to ATA33, a normal 40-pin, 1.27mm-pitch conductor cable is sufficient. Higher transfer rates such as ATA66 and ATA100 require 80-pin conductor cables, where the extra 40 conductors are tied to ground to isolate the adjacent signals for better signal integrity. The 80-pin cable assembly also ties pin 34 (IDE_CBLID#) on the 40-pin header to GND. If IDE_CBLID# is sampled low by the Module's BIOS, it assumes that the proper high-speed cable is present and sets up the drive parameters accordingly. Jumper settings on the IDE devices determine Master/Slave configuration. The drive activity LED is driven by the Module's pin A28 (COM Express pin ATA_ACT#).

Figure 24: Connector type: 40 pin, 2 row 2.54mm grid female



2.10.3. IDE 44-Pin Header (2.5 Inch and Low Profile Optical Drives)

To interface standard 2.5-inch parallel ATA drives, as well as low profile optical drives, a standard 2.0mm, two row, 44-pin connector in combination with a 44-conductor ribbon cable is used. For slower drive speeds up to ATA33, a normal 44-conductor, 1.0mm-pitch cable is sufficient. Higher transfer rates such as ATA66 and ATA100 require special handling as ground isolated cables like those commonly used for 3.5” ATA devices do not exist for this interface. Simulation as well as testing should be used to determine if an application specific 44-pin cable interface can support ATA66 and ATA100 speeds. Items to be taken into consideration include cable length, placement in the system, folds and routing. Because 44-conductor cables have no method of indicating their transfer rate capability, IDE_CBLID# must be controlled on the carrier board or by using BIOS setup. For 44-pin ATA devices, the drive activity LED is driven by pin 39 of the header.

2.10.4. CompactFlash 50 Pin Header

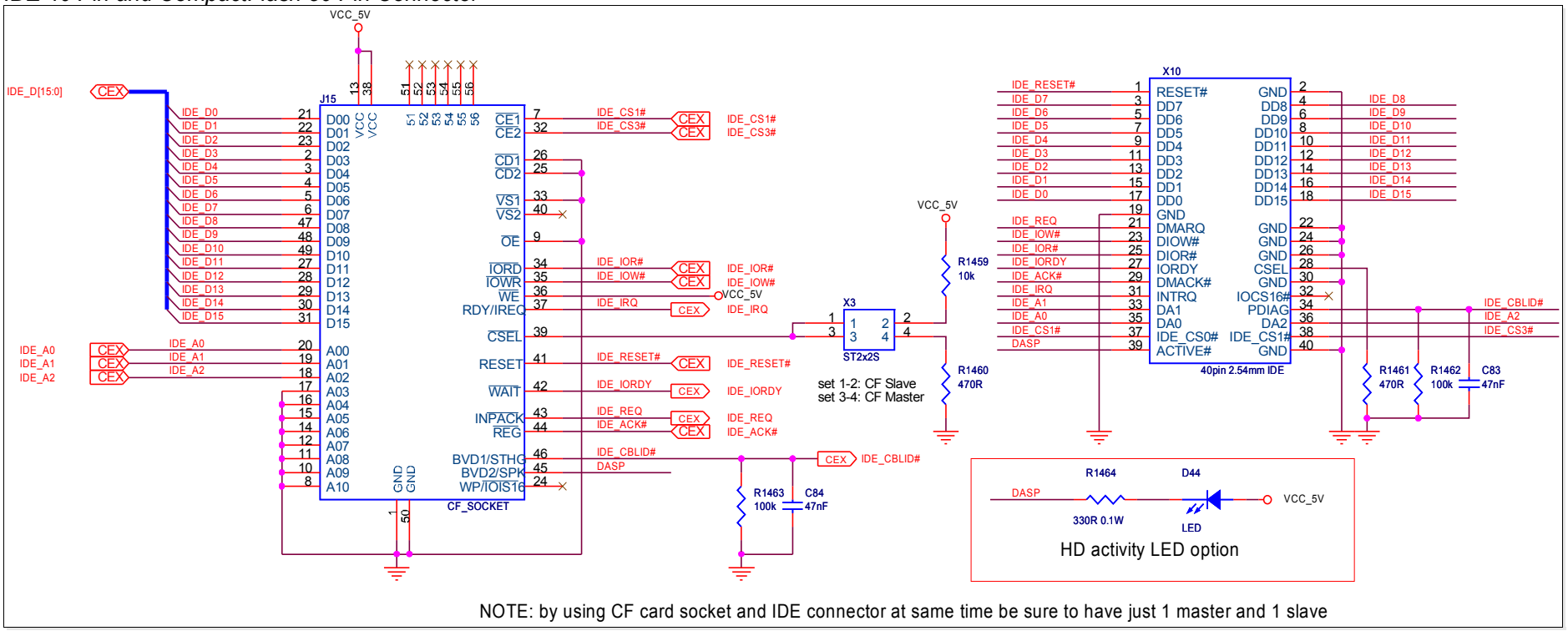
CompactFlash (CF) cards with DMA capability require that the two signals 'IDE_REQ' and 'IDE_ACK#' are routed to the CF card socket on the COM Express Carrier Board. If this is not done then some DMA capable CF cards may not work because they are not designed for non DMA mode. For more information about this subject, refer to the data sheet of the CF card or contact your CF card manufacturer.

CF socket pin 39 (CSEL#) is connected to a jumper to select Master or Slave configuration. If jumpered low, the drive is configured for Master mode. This provides the ability to perform a CompactFlash boot.

2.10.5. IDE / CompactFlash Reference Schematics

This reference schematic shows a circuitry implementing an IDE connector and a CF card socket that is DMA capable.

Figure 25: IDE 40 Pin and CompactFlash 50 Pin Connector



NOTE: by using CF card socket and IDE connector at same time be sure to have just 1 master and 1 slave

2.10.6. Routing Considerations

The IDE signals are single-ended signals with a nominal impedance of 55 Ω. See Section 6.5.2. 'IDE Trace Routing Guidelines' on page 141 for more information about routing considerations.

2.11. VGA

2.11.1. Signal Definitions

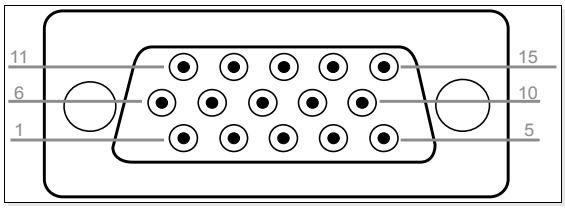
The COM Express Specification defines an analog VGA RGB interface for all Module types. The interface consists of three analog color signals (Red, Green, Blue); digital Horizontal and Vertical Sync signals as well as a dedicated I2C bus for Display Data Control (DDC) implementation for monitor capability identification. The corresponding signals can be found on the COM Express Module connector row B.

Table 23: VGA Signal Description

Signal	Pin	HDSUB15	Description	I/O	Comment
VGA_RED	B89	1	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_GRN	B91	2	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_BLU	B92	3	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_HSYNC	B93	13	Horizontal sync output to VGA monitor.	O 3.3V CMOS	
VGA_VSYNC	B94	14	Vertical sync output to VGA monitor.	O 3.3V CMOS	
VGA_I2C_CK	B95	15	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V CMOS	
VGA_I2C_DAT	B96	12	DDC data line.	I/O 3.3V CMOS	
GND		5..8, 10	Analog and Digital GND		
DDC_POWER		9	5V DDC supply voltage for monitor EEPROM		Power
N.C.		4, 11	Not Connected		

2.11.2. VGA Connector

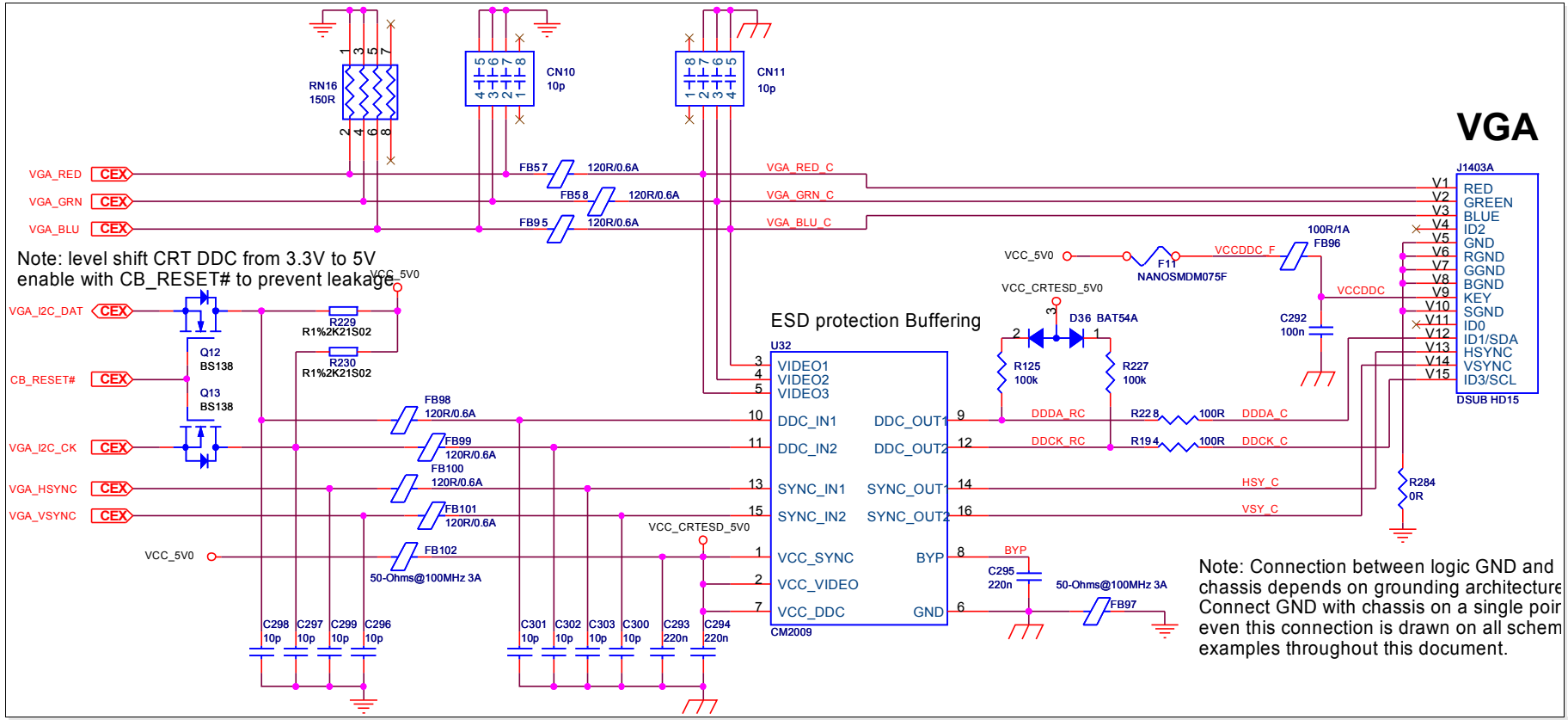
Figure 26: VGA Connector HDSUB15



2.11.3. VGA Reference Schematics

This reference schematic shows a circuitry implementing a VGA port.

Figure 27: VGA Reference Schematics



2.11.4. Routing Considerations

2.11.4.1. RGB Analog Signals

The RGB signal interface of the COM Express Module consists of three identical 8-bit digital-to-analog converter (DAC) channels. One each for the red, green, and blue components of the monitor signal. Each of these channels should have a 150Ω ±1% pull-down resistor connected from the DAC output to the Carrier Board ground. A second 150Ω ±1% termination resistor exists on the COM Express Module itself. An additional 75Ω termination resistor exists within the monitor for each analog DAC output signal.

Since the DAC runs at speeds up to 350MHz, special attention should be paid to signal integrity and EMI. There should be a PI-filter placed on each RGB signal that is used to reduce high-frequency noise and EMI. The PI-filter consists of two 10pF capacitors with a 120Ω @ 100MHz ferrite bead between them. It is recommended to place the PI-filters and the terminating resistors as close as possible to the standard VGA connector.

2.11.4.2. HSYNC and VSYNC Signals

The horizontal and vertical sync signals 'VGA_HSYNC' and 'VGA_VSYNC' provided by the COM Express Module are 3.3V tolerant outputs. Since VGA monitors may drive the monitor sync signals with 5V tolerance, it is necessary to implement high impedance unidirectional buffers. These buffers prevent potential electrical over-stress of the Module and avoid that VGA monitors may attempt to drive the monitor sync signals back to the Module.

For optimal ESD protection, additional low capacitance clamp diodes should be implemented on the monitor sync signals. They should be placed between the 5V power plane and ground and as close as possible to the VGA connector.

2.11.4.3. DDC Interface

COM Express provides a dedicated I2C bus for the VGA interface. It corresponds to the VESA™ defined DDC interface that is used to read out the CRT monitor specific Extended Display Identification Data (EDID™). The appropriate signals 'VGA_I2C_DAT' and 'VGA_I2C_CK' of the COM Express Module are supposed to be 3.3V tolerant. Since most VGA monitors drive the internal EDID™ EEPROM with a supply voltage of 5V, the DDC interface on the VGA connector must also be sourced with 5V. This can be accomplished by placing a 100kΩ pull-up resistors between the 5V power plane and each DDC interface line. Level shifters for the DDC interface signals are required between the COM Express Module signal side and the signals on the standard VGA connector on the Carrier Board.

Additional Schottky diodes must be placed between 5V and the pull-up resistors of the DDC signals to avoid backward current leakage during Suspend operation of the Module.

2.11.4.4. ESD Protection/EMI

All VGA signals need ESD protection and EMI filters. This can be provided by using a VGA port companion circuit or similar protective components. The Carrier Board sample VGA schematic shown above uses a “VGA companion” protection circuit, the CM2009 from California Micro Devices. The companion circuit implements ESD protection for the analog DAC output, DDC and SYNC signals through the use of low-capacitance current steering diodes. Additionally, it incorporates level shifting for the DDC signals and buffering for the SYNC signals. For more details, refer to the 'CM2009' data sheet.

Many other protection and level shifting solutions are possible. Semtech offers a wide variety of low capacitance ESD suppression parts suitable for high speed signals. One such Semtech part is the RCLAMP502B.

2.12. TV-Out

2.12.1. Signal Definitions

TV-Out signals are defined on COM Express connector row B. Up to Module 3 individual digital-to-analog converter (DAC) channels are available on the connector. The following video formats may be supported:

Composite Video: All color, brightness, blanking, and sync information are encoded onto a single signal.

S-Video: (Separated Video) video signal with two components, brightness (luma) and color (chroma). This is also known as Y-C video.

Component Video: A video signal that consists of three components. The components may be RGB or may be encoded using other component encoding schemes such as YUV, YCbCr, and YPbPr.

A COM Express Module may support all, some, or none of these formats. Within these formats, there are different encoding schemes that may be used. The most widely used encoding schemes are NTSC (used in primarily in North America) and PAL (used primarily in Europe)

Which format and encoding options are available are Module and vendor dependent. Only one output mode can be used at any given time.

Table 24: TV-Out Signal Definitions

Signal	Pin	Description	I/O	Comment
TV_DAC_A	B97	TV-DAC channel A output supporting: **Composite video**: CVBS **Component video**: Chrominance (Pb) **S-Video**: not used	O Analog	Analog output
TV_DAC_B	B98	TV-DAC channel B output supporting: **Composite video**: not used **Component video**: Luminance (Y) **S-Video**: Luminance (Y)	O Analog	Analog output
TV_DAC_C	B99	TV-DAC channel C output supporting: **Composite video**: not used **Component**: Chrominance (Pr) **S-Video**: Chrominance (C)	O Analog	Analog output

2.12.2. TV-Out Connector

Figure 28: TV-Out Video Connector (combined S-Video and Composite)

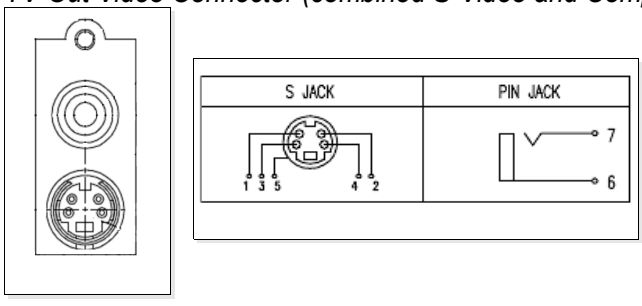


Table 25: TV-Out Connector Pinout

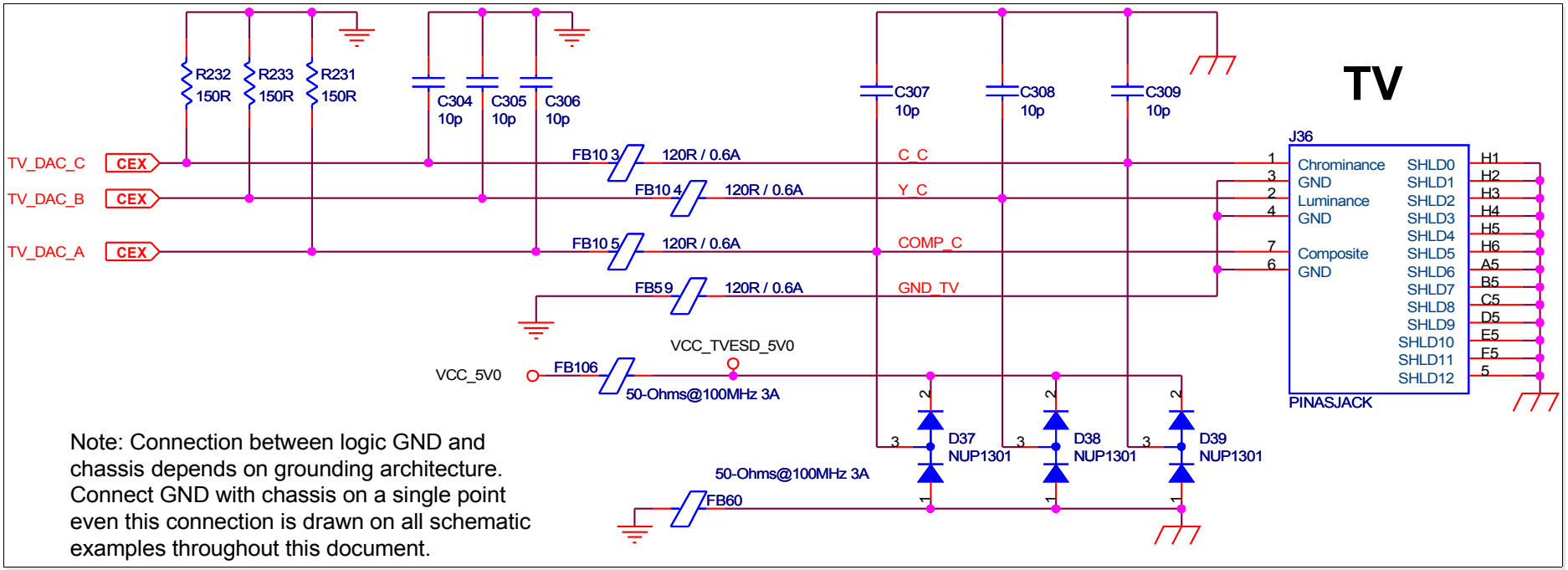
Pin	Signal	Description	Pin	Signal	Description
1	Chrominance (C)	S-Video Chrominance Analog Signal (C)	2	Luminance (Y)	S-Video Luminance Analog Signal (Y)
3	GND (C)	Analog Ground for Chrominance (C)	4	GND (Y)	Analog Ground Luminance (Y)
5	GND	Analog Ground	6	GND	Analog Ground
7	Composite	Composite Video Output			

2.12.3. TV-Out Reference Schematics

All signals along the left edge of the figure below are sourced directly from the COM Express Module. No additional pull-ups or terminations beyond what is shown in the figure are required.

The 150 Ω termination to ground is important both for signal integrity and to establish the correct DC level on the line. All components shown in this figure should be placed close to the Carrier Board connector shown in the figure.

Figure 29: TV-Out Reference Schematics



2.12.4. Routing Considerations

At least 30mils of spacing should be used for the routing between each TV-DAC channel to prevent crosstalk between the TV-DAC signals. The maximum trace length distance of the TV-DAC signals between the COM Express connector and the 150Ω ±1% termination resistor should be within 12 inches. This distance should be routed with a 50Ω trace impedance.

2.12.4.1. Signal Termination

Each of the TV-DAC channels should have a 150Ω ±1% pull-down termination resistor connected from the TV-DAC output of the COM Express Module to the Carrier Board ground. This termination resistor should be placed as close as possible to the TV-Out connector on the Carrier Board. A second 150Ω ±1% termination resistor exists on the COM Express Module itself.

2.12.4.2. Video Filter

There should be a PI-filter placed on each TV-DAC channel output to reduce high-frequency noise and EMI. The PI-filter consists of two 10pF capacitors with a 120Ω @ 30Mhz ferrite bead between them. It is recommended to place the PI-filters and the termination resistors as close as possible to the TV-Out connector on the Carrier Board. The PI-filters should be separated from each other by at least 50mils or more in order to minimize crosstalk between the TV-DAC channels.

2.12.4.3. ESD Protection

ESD clamp diodes are required for each TV-DAC channel. These low capacitance clamp diodes should be placed as near as possible to the TV-Out connector on the COM Express Carrier Board between +5V supply voltage and ground.

2.13. AC'97 and HDA Digital Audio Interfaces

The COM Express Specification allocates seven pins on the A-B connector to support digital AC’97 and HD interfaces to audio Codecs on the Carrier Board. The pins are available on all Module types. High-definition (HD) audio uses the same digital-signal interface as AC ’97 audio. Codecs for AC ’97 and HD Audio are different.

2.13.1. Signal Definitions

Table 26: Audio Codec Signal Descriptions

Signal	Pin	Description	I/O	Comment
AC_RST#	A30	CODEC Reset.	O 3.3V Suspend CMOS	
AC_SYNC	A29	Serial Sample Rate Synchronization.	O 3.3V CMOS	
AC_BITCLK	A32	12.228 MHz Serial Bit Clock for CODEC.	O 3.3V CMOS	
AC_SDOUT	A33	Audio Serial Data Output Stream.	O 3.3V CMOS	
AC_SDIN0 AC_SDIN1 AC_SDIN2	B30 B29 B28	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS	

Information about which audio interface is supported on the COM Express Module can be found in the corresponding COM Express Module's user's guide. On COM Express Modules that support the AC'97 Digital Interface only, it is not possible to use HDA codecs.

Some COM Express Modules support both the AC'97 and HDA Interface. In these cases the COM Express Module's 'BIOS Setup Program' offers a setup entry to choose which interface should be utilized. Only audio codecs that match this setting will work properly. AC’97 and High Definition Audio codecs cannot be mixed on the same link or behind the same controller.

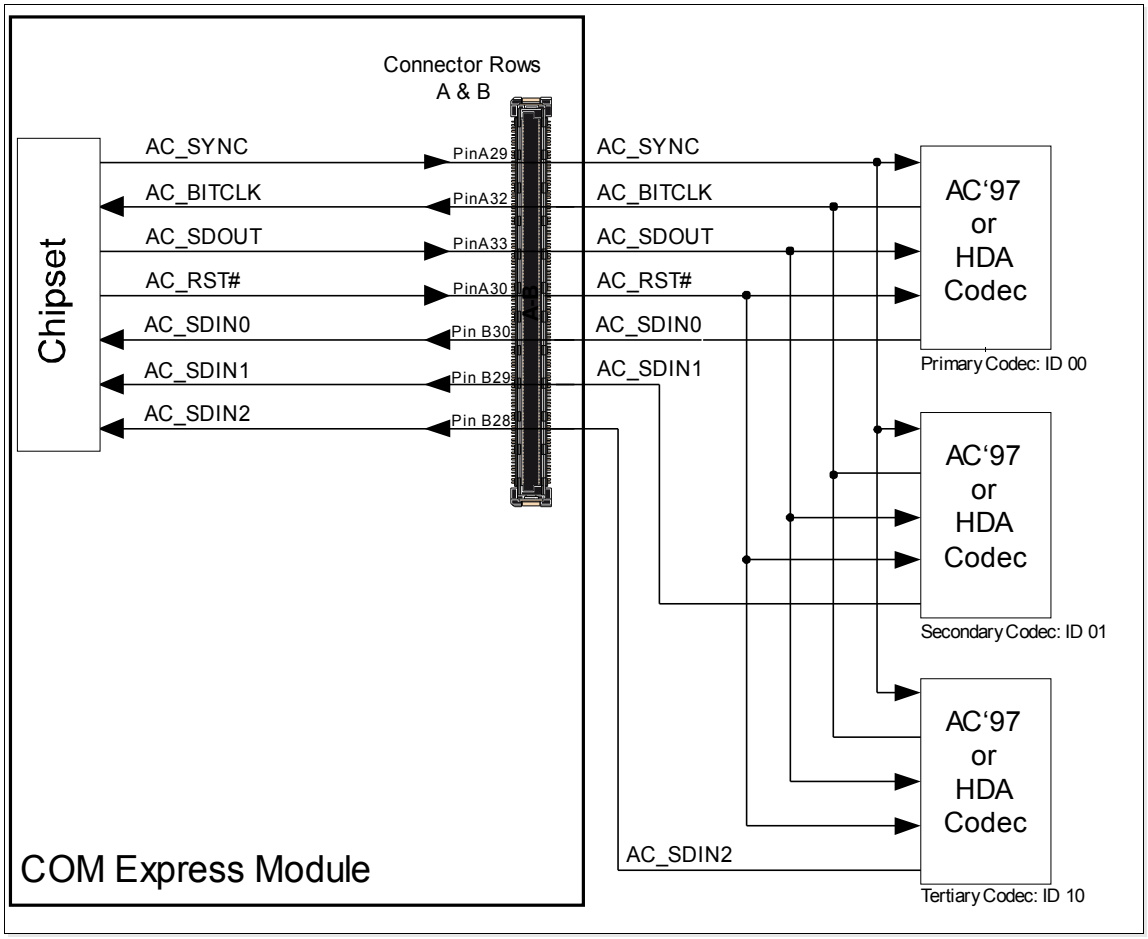
The AC'97 or HDA codec on a COM Express Carrier Board is usually connected as the primary codec with the codec ID 00 using the data input line 'AC_SDIN0'. Up to two additional codecs with ID 01 and ID 10 can be connected to the COM Express Module by using the other designated signals 'AC_SDIN1' and 'AC_SDIN2'.

Connect the primary audio codec to the serial data input signal 'AC_SDIN0' and ensure that the corresponding bit clock input signal 'AC_BITCLK' is connected to the AC'97/HDA interface of the COM Express Module.

Clocking over the signal 'AC_BITCLK' is derived from a 24.576 MHz crystal or crystal oscillator provided by the primary codec in AC97 implementations. The crystal is not required in HDA implementations This clock also drives the second and the third audio codec if more than one codec is used in the application. For crystal or crystal oscillator requirements, refer to the datasheet of the primary codec.

Note ***Intel 915GM and 945GM chipsets support both AC97 and HDA formats in the silicon. Intel 965GM and later mobile chipsets support HDA only.***

Figure 30: Multiple Audio Codec Configuration



2.13.2. Reference Schematics

2.13.2.1. AC'97

Figure 31: AC'97 Schematic Example

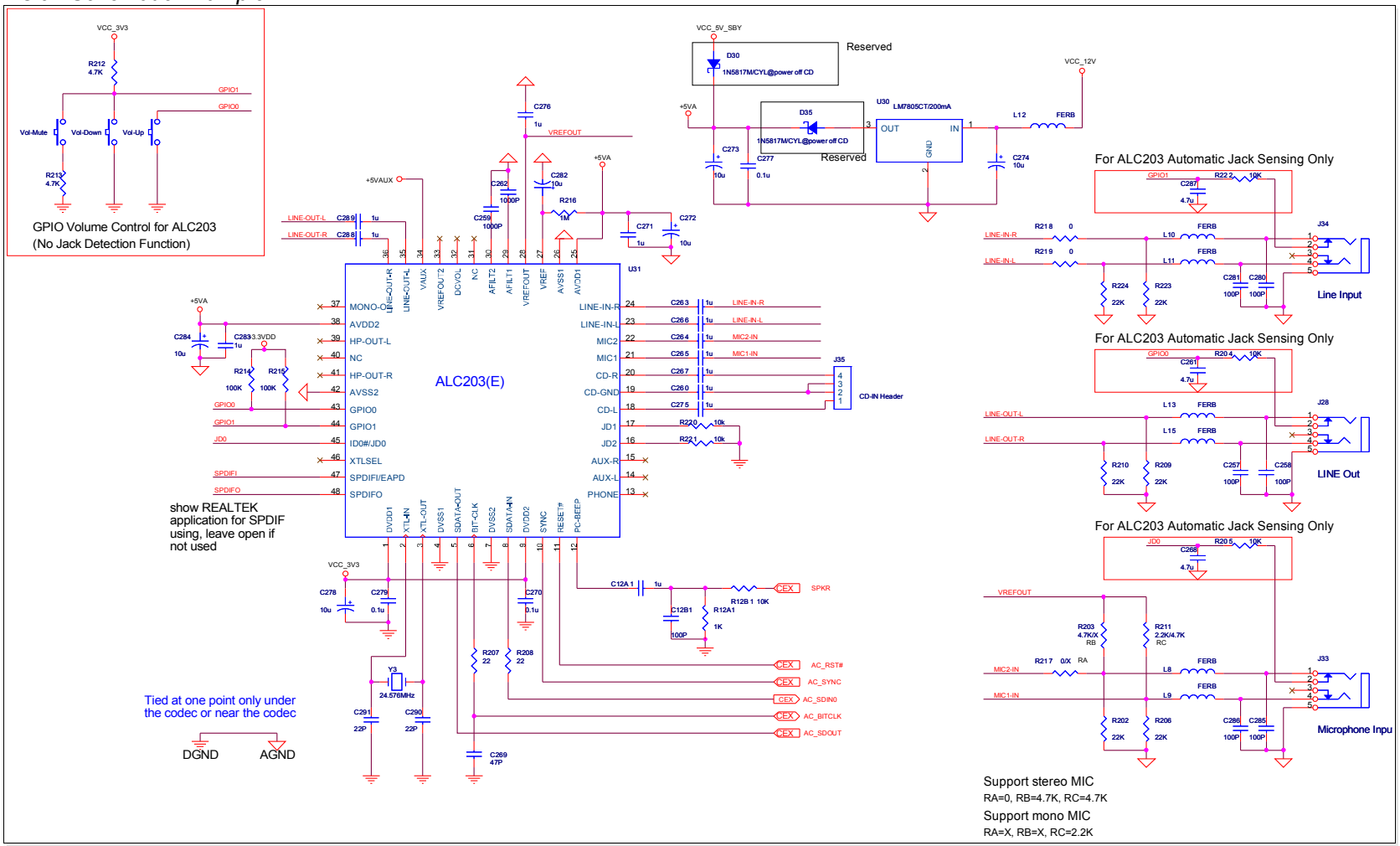
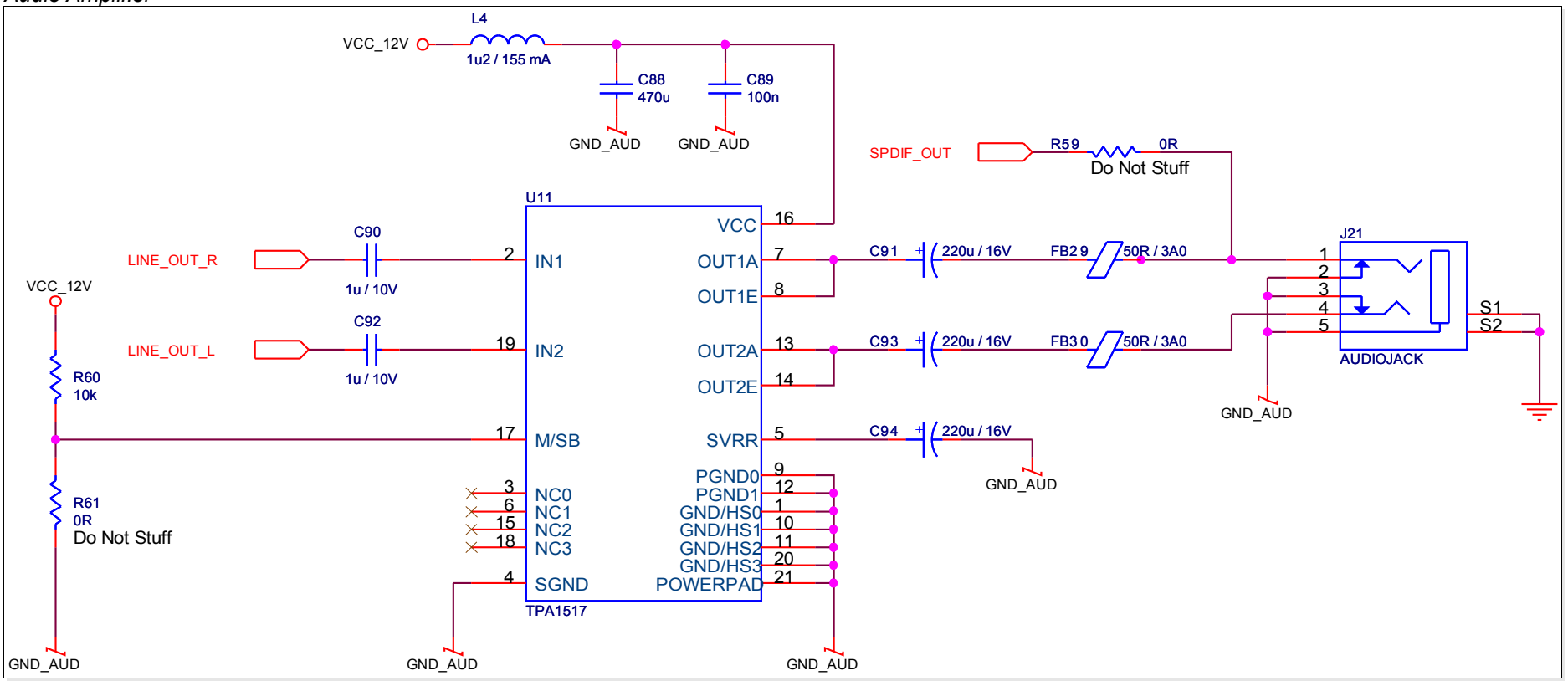
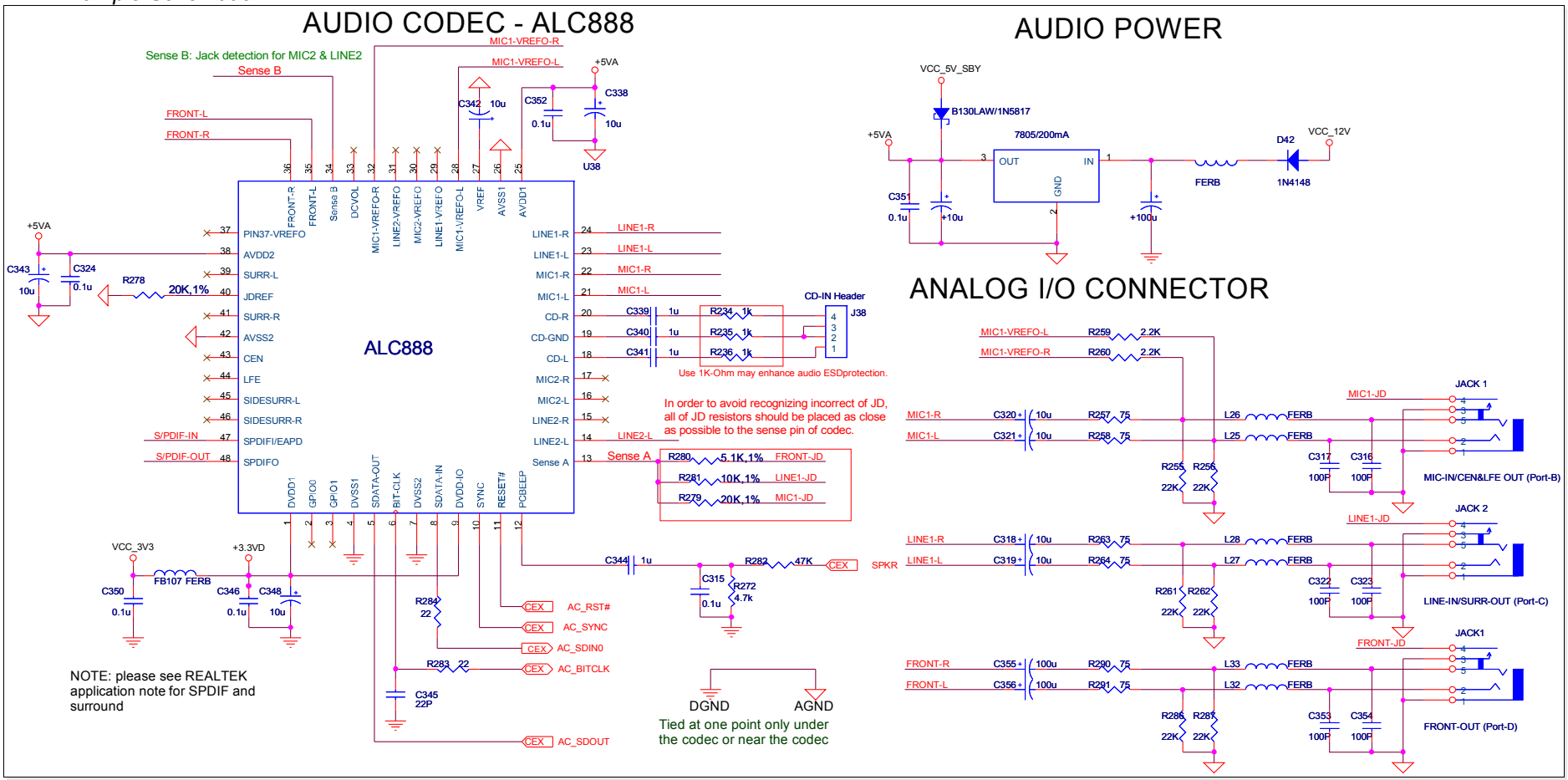


Figure 32: Audio Amplifier



2.13.2.2. High Definition Audio (HDA)

Figure 33: HDA Example Schematic



2.13.3. Routing Considerations

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies and analog ground planes from the rest of the Carrier Board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

Traces must be routed with a target impedance of 55Ω with an allowed tolerance of ±15%.

Ground return paths for the analog signals must be given special consideration.

Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.

Partition the Carrier Board with all analog components grouped together in one area and all digital components in another.

Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05 inch wide.

Route analog power and signal traces over the analog ground plane.

Route digital power and signal traces over the digital ground plane.

Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.

Place the crystal or oscillator (depending on the codec used) as close as possible to the codec. (HDA implementations generally do not require a crystal at the codec)

Do not completely isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05 inch wide.

Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. That is, no signal should cross the split/gap between the ground planes, because this would cause a ground loop, which in turn would greatly increase EMI emissions and degrade the analog and digital signal quality.

2.14. PCI Bus

2.14.1. Signal Definitions

Type 2 and 3 COM Express Modules provide a 32-bit PCI bus that can operate up to 33 MHz. The corresponding signals can be found on the Module connector rows C and D.

Table 27: PCI Bus Signal Definition

Signal	Pin#	Description	I/O	Comment
PCI_AD0	C24	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD1	D22	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD2	C25	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD3	D23	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD4	C26	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD5	D24	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD6	C27	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD7	D25	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD8	C28	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD9	D27	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD10	C29	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD11	D28	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD12	C30	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD13	D29	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD14	C32	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD15	D30	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD16	D37	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD17	C39	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD18	D38	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD19	C40	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD20	D39	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 0
PCI_AD21	C42	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 1
PCI_AD22	D40	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 2
PCI_AD23	C43	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 3
PCI_AD24	D42	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD25	C45	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD26	D42	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD27	C46	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD28	D44	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD29	C47	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD30	D45	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD31	C48	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_C/BE0#	D26	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE1#	C33	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE2#	C38	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE3#	C44	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_DEVSEL#	C36	PCI bus Device Select, active low	I/O 3.3V	
PCI_Frame#	D36	PCI bus Frame control line, active low	I/O 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low	I/O 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low	I/O 3.3V	

Signal	Pin#	Description	I/O	Comment
PCI_STOP#	D34	PCI bus STOP control line, active low	I/O 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V	
PCI_PERR#	C34	Parity Error: An external PCI device drivers PERR# by driving it low, when it receives data that has a parity error.	I/O 3.3V	
PCI_REQ0#	C22	PCI bus master request input line, active low	I 3.3V	
PCI_REQ1#	C19	PCI bus master request input line, active low	I 3.3V	
PCI_REQ2#	C17	PCI bus master request input line, active low	I 3.3V	
PCI_REQ3#	D20	PCI bus master request input line, active low	I 3.3V	
PCI_GNT0#	C20	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT1#	C18	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT2#	C16	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT3#	D19	PCI bus master grant output line, active low	O 3.3V	
PCI_RESET#	C23	PCI Reset output, active low	O 3.3V_SBY	Asserted during system reset
PCI_LOCK#	C35	PCI Lock control line, active low	I/O 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition	I/O 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to low to wake up the system from low-power states S1-S5	I 3V3_SBY	
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	
PCI_IRQA#	C49	PCI interrupt request line A	I 3.3V	
PCI_IRQB#	C50	PCI interrupt request line B	I 3.3V	
PCI_IRQC#	D46	PCI interrupt request line C	I 3.3V	
PCI_IRQD#	D47	PCI interrupt request line D	I 3.3V	
PCI_CLK	D50	PCI 33MHz clock output	O 3.3V	
PCI_M66EN	D49	Module input signal that indicates whether a Carrier Board PCI device is capable of 66MHz operation. It is pulled to ground by Carrier Board device or by slot card, if one of the devices is NOT capable of 66MHz operation.	I 3.3V	

2.14.2. Reference Schematics

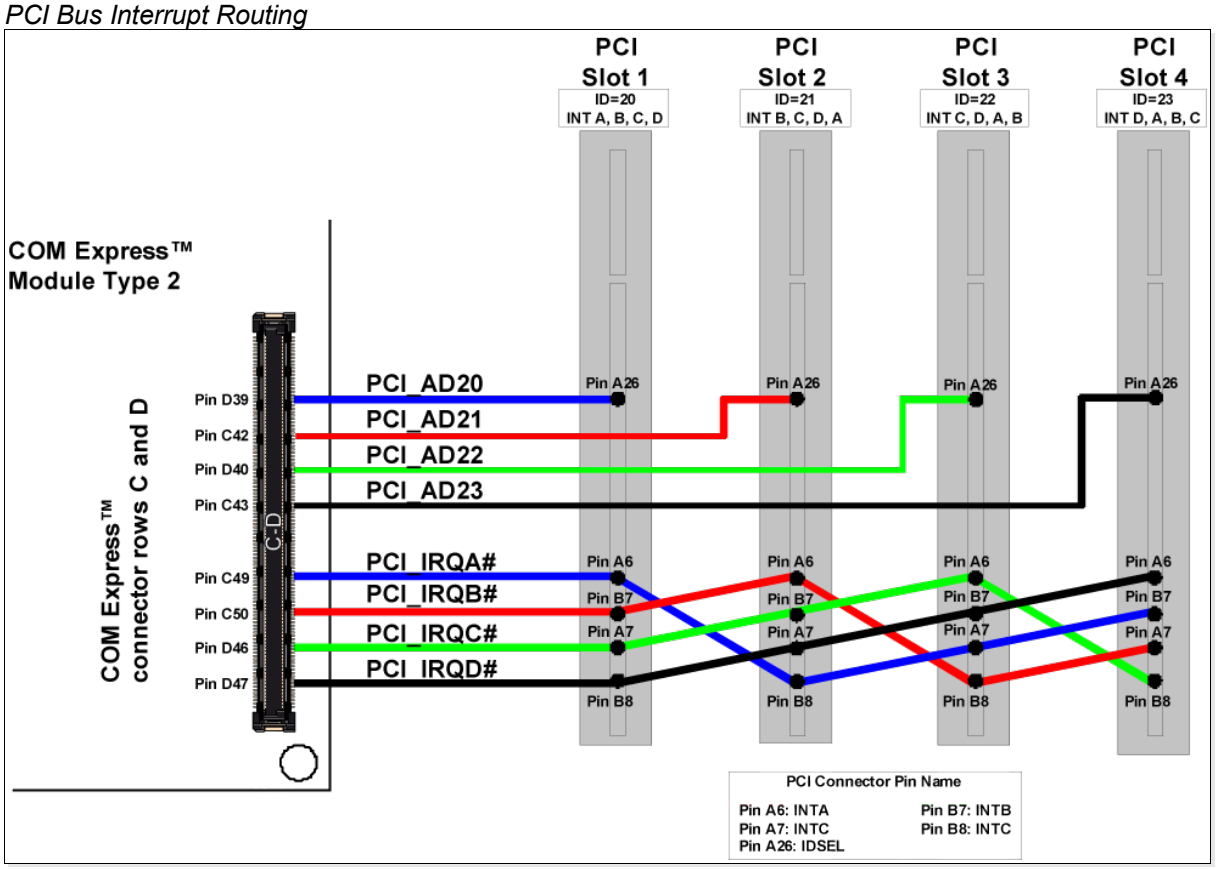
2.14.2.1. Resource Allocation

The COM Express PCI interface is compliant to the 'PCI Local Bus Specification Revision 2.3'. It supports up to four bus master capable PCI bus slots or external PCI devices designed on the COM Express Carrier Board. The PCI interface is specified to be +5V tolerant, with +3.3V signaling. All necessary PCI bus pull-up resistors must be included on the COM Express Module.

Allocate PCI resources (IDSEL pin assignments, interrupts, request lines and grant lines) per Figure 34 below. The PCI Specification requires that PCI devices be capable of sharing interrupts. Interrupt latency is reduced if devices do not share interrupts; hence the interrupt “rotation” scheme shown below is recommended. If there are more than four PCI devices in the system, then some interrupt-sharing is inevitable.

The signal 'IDSEL' of each external PCI device or PCI slot has to be connected through a 22Ω resistor to a separate PCI address line. For PCI bus slots 1-4, COM Express specifies the PCI address lines AD[20] to AD[23].

Figure 34: PCI Bus Interrupt Routing



Most of these PCI devices only utilize the interrupt signal 'INTA#'. To distribute the interrupt source of the devices over the interrupt signals 'INTB#', 'INTC#' and 'INTD#', an interrupt cross routing scheme has to be implemented on the COM Express Carrier Board design. Figure 34 above and Table 28 below illustrate the PCI bus interrupt routing for the PCI bus slots 1-4.

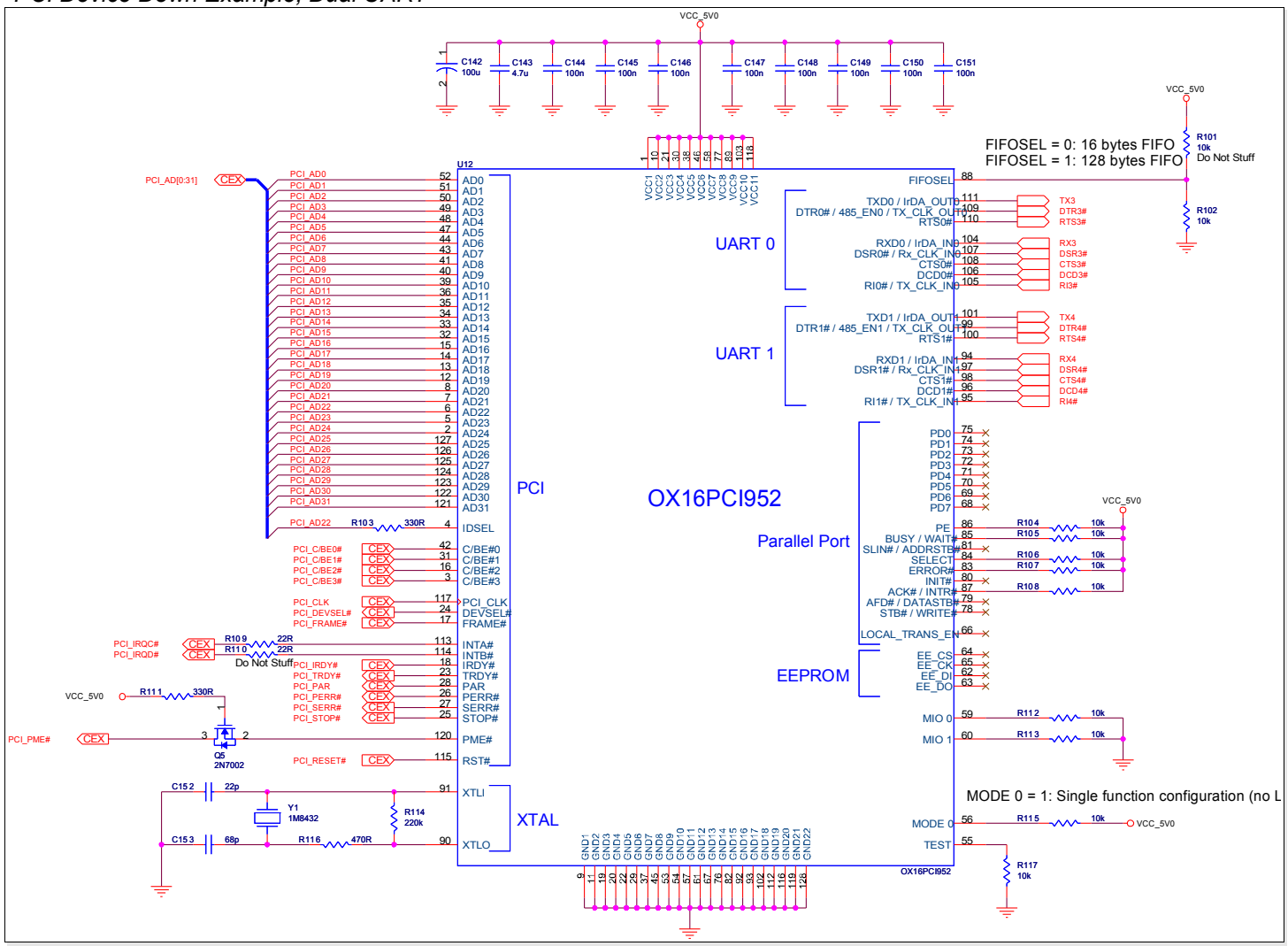
Table 28: PCI Bus Interrupt Routing

Device Signal	Slot / Device 1	Slot / Device 2	Slot / Device 3	Slot / Device 4
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTC# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#

Requests and Grants cannot be shared. There should only be a single REQ / GNT pair per device.

2.14.2.2. Device-Down Example

Figure 35: PCI Device Down Example; Dual UART

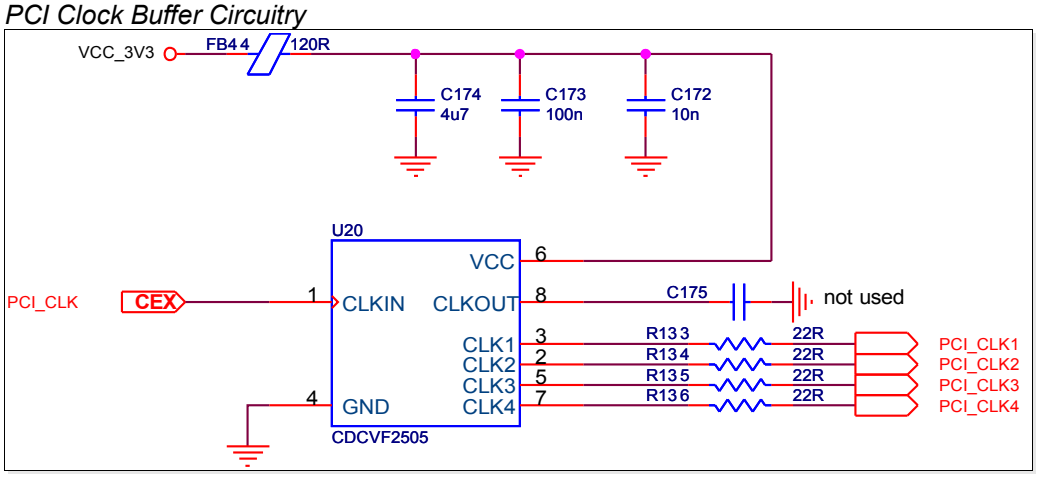


2.14.2.3. Device-Down Considerations

2.14.2.4. Clock Buffer

The COM Express Specification only supports a single PCI clock signal called 'PCI_CLK' to be used on the Carrier Board. If there are multiple devices or slots implemented on the Carrier Board, a zero delay clock buffer is required to expand the number of PCI clocks so that each device or each bus slot will be provided with a separate clock signal. Figure 36 below shows an example using the Texas Instruments 'CDCVF2505' zero delay clock buffer providing four output clock signals with spread spectrum compatibility (http://www.ti.com).

Figure 36: PCI Clock Buffer Circuitry



Note: In accordance with the 'PCI Local Bus Specification Revision 2.3', the PCI clock signal requires a rise and fall time (slew rate) within 1V/ns and 4V/ns. The slew rate must be met across the minimum peak-to-peak portion of the clock wave form, which is between 0.66V and 1.98V for 3.3V clock signaling. These parameters are very critical for EMI and must be observed during Carrier Board layout when implementing the PCI Bus.

2.14.3. Routing Considerations

2.14.3.1. General PCI Signals

Route the PCI bus with 55-Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane, or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

See Section 6.5.1. 'PCI Trace Routing Guidelines' on page 140 for a summary of trace routing parameters and guidelines.

2.14.3.2. PCI Clock Routing

Particular attention must be paid to the PCI clock routing. The PCI Local Bus specification requires a maximum propagation delay for the clock signals of 10ns within a propagation skew of 2ns @ 33MHz between the several clock signals.

The COM Express Specification allows 1.6ns ± 0.1ns @ 33MHz propagation delay for the PCI clock signal beginning from the Module pin to the destination pin of the PCI device. The propagation delay is dependent on the trace geometries, PCB stack-up and the PCB dielectric constant.

Calculating using a typical propagation delay value of 180ps/inch for an internal layer clock trace of the Carrier Board, a maximum trace length of 8.88 inches is allowed.

The clock trace from the COM Express Module to a PCI bus slot should be 2.5 inches shorter because PCI cards are specified to have 2.5 inches of clock trace length on the card itself.

PCI clock signals should be routed as a single ended trace with a trace impedance of 55Ω. To reduce EMI, a single ground referenced internal layer is recommended. The clock traces should be separated as far as possible from other signal traces.

Refer to Section 6.5.1 'PCI Trace Routing Guidelines' on page 140 below and the 'PCI Local Bus Specification Revision 2.3' to get more information about this subject.

Note: ***An approximate value for the signal propagation delay per trace length inch can be calculated by using the following formula:***

$$t_{prop.} = \frac{\sqrt{\varepsilon_r'}}{11.8}\frac{ns}{inch}$$

ε_r' can be determined from the dielectric constant of the PCB that is used by the following approximation. A typical value for the dielectric constant of an FR4 PCB material is 4.2 < ε_r < 4.5.

For stripline routing: $\varepsilon_r' = \varepsilon_r$

For microstrip routing: $\varepsilon_r' = 0.475\,\varepsilon_r + 0.67 \quad for \quad 2.0 < \varepsilon_r < 6.0$

2.15. LPC Bus – Low Pin Count Interface

Since COM Express is designed to be a legacy free standard for embedded Modules, it does not support legacy functionality on the Module, such as PS/2 keyboard/mouse, serial ports, and parallel ports. Instead, it provides an LPC interface that can be used to add peripheral devices to the Carrier Board design. COM Express also provides interface pins necessary for (optional) Carrier Board resident PS keyboard controllers

The Low Pin Count Interface was defined by the Intel® Corporation to facilitate the industry's transition toward legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface Firmware Hubs, Trusted Platform Module (TPM) devices, general-purpose inputs and outputs, and Embedded Controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. It is straightforward to develop PLDs or FPGAs that interface to the LPC bus. A PLD circuit example is given in Figure 39 'LPC PLD Example – Port 80 Decoder Schematic' below.

For more information about LPC bus, refer to the 'Intel® Low Pin Count Interface Specification Revision 1.1'.

2.15.1. Signal Definition

Table 29: LPC Interface Signal Descriptions

Signal	Pin	Description	I/O	Comment
LPC_SERIRQ	A50	LPC serialized IRQ.	I/O 3.3V CMOS	
LPC_FRAME#	B3	LPC frame indicates start of a new cycle or termination of a broken cycle.	O 3.3V CMOS	
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed command, address and data.	I/O 3.3V CMOS	
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC encoded DMA/Bus master request.	I 3.3V CMOS	Not all modules support LPC DMA. Contact your vendor for information.
LPC_CLK	B10	LPC clock output 33MHz.	O 3.3V CMOS	

Note ***Implementing external LPC devices on the COM Express Carrier Board always requires customization of the COM Express Module's BIOS in order to support basic initialization for those LPC devices. Otherwise the functionality of the LPC devices will not be supported by a Plug&Play or ACPI capable system. See Section 4 'BIOS Considerations' on page 124 below for further information. Contact your module vendor for a list of specific SIO devices for which there may be BIOS support.***

2.15.2. LPC Bus Reference Schematics

2.15.2.1. LPC Bus Clock Signal

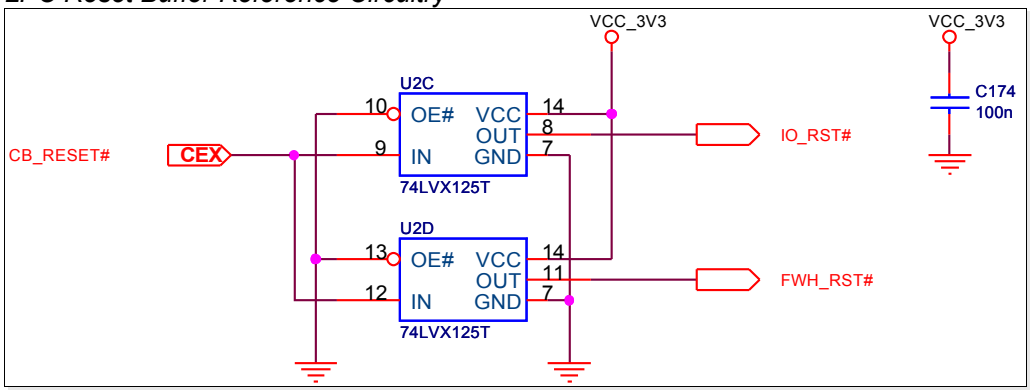
COM Express specifies a single LPC reference clock signal called 'LPC_CLK' on the Modules connector at row B pin B10. Newer chipsets do not provide a free running LPC_CLK. The clock is stopped and started on-the-fly. The clock is only active during LPC bus cycles. This kind of a clock can cause problems when used with PLL based zero delay buffers which require a number of clock cycles to lock onto the incoming clock before the output is active. The issue is that the LPC_CLK is not active for enough cycles before the data is read/written to the LPC bus. The result is that the target LPC device does not see an LPC_CLK and misses the LPC cycle.

Carrier designers should not buffer LPC_CLK for maximum Module interoperability. The COM Express specification intends for a single load on the clock but experience has shown that two devices can be driven if both devices are within 2" of each other.

2.15.2.2. LPC Reset Signal

The LPC interface should use the signal 'CB_RESET#' as its reset input. This signal is issued by the COM Express Module as a result of a low 'SYS_RESET#', a low 'PWR_OK' or a watchdog timeout event. If there are multiple LPC devices implemented on the Carrier Board, it is recommended to split the signal 'CB_RESET#' so that each LPC device will be provided with a separate reset signal. Therefore a buffer circuit like the one shown in Figure 37 below should be used.

Figure 37: LPC Reset Buffer Reference Circuitry

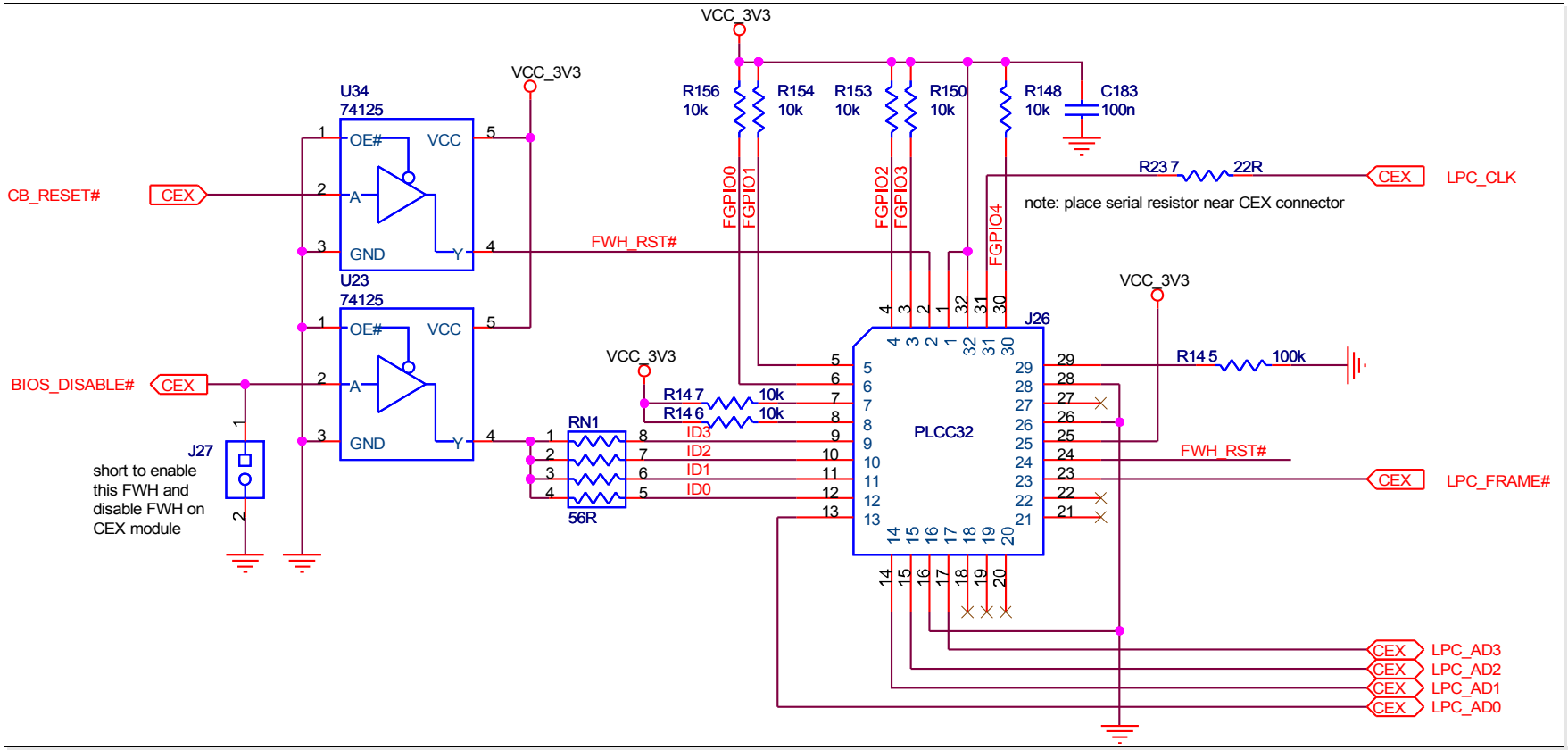


2.15.2.3. LPC Firmware Hub

An example of a Carrier Board Firmware Hub (FWH) implementation is shown in Figure 38 below. Use the FWH to store and execute BIOS code.

A feature of the COM Express specification is the inclusion of the BIOS_DISABLE# pin. If this pin is pulled low on the Carrier Board, then the BIOS on the Module is disabled. The BIOS can instead reside on the Carrier Board LPC or PCI buses. This is useful in some regulatory situations in which it is required that regulatory technicians remove the BIOS, check its integrity, and replace it. There is usually room on a Carrier Board for a socketed BIOS, whereas the Module BIOS is often a surface-mount device. The use of this feature is illustrated in the example below.

Figure 38: LPC Firmware Hub



The BIOS device shown in Figure 38 above is a SST SST49LF008A Firmware Hub in a 32-pin PLCC package. The socket used is a 32-pin PLCC socket, AMP/Tyco 822498-1. This is a surface-mount socket, and PCBs can be laid out such that the socket or the FWH itself is soldered to the Carrier Board.

The FWH is connected to the system via the LPC interface. Data and address information are carried on the LPC_AD[0:3] lines. LPC_FRAME indicates the start of a new frame.

FWH pins 2 (RST#) and 24 (INIT#) reset the FWH. These pins are logically combined together internally on the FWH, and a low on either pin will reset the FWH.

FWH pins 6, 5, 4, 3, 30 – (FGPI [0:4]) are general-purpose inputs that may be read by system software. They should be tied to a valid logic level.

FWH pin 7 (WP#) enables write protection for main block sectors when it is pulled low. If pulled high, hardware write protection is disabled. FWH pin 8 (TBL#) enables write protection for the top block sector when pulled low.

FWH pins 12,11,10, 9 – (ID[0:3]) are ID pins that allow multiple FWH parts (up to 16) to be used. By convention, in Intel x86-based systems, the boot device is FWH number 0. To boot from the Carrier Board FWH, the Module BIOS_DISABLE# pin must be low (to disable the Module BIOS) and the Carrier Board FWH ID[0:3] pins (pins 12,11,10,9) must be low (to enable it as the boot device). If jumper J27 in Figure 38 above is installed, the Module BIOS is disabled, and the Carrier Board FWH may be used as a boot device.

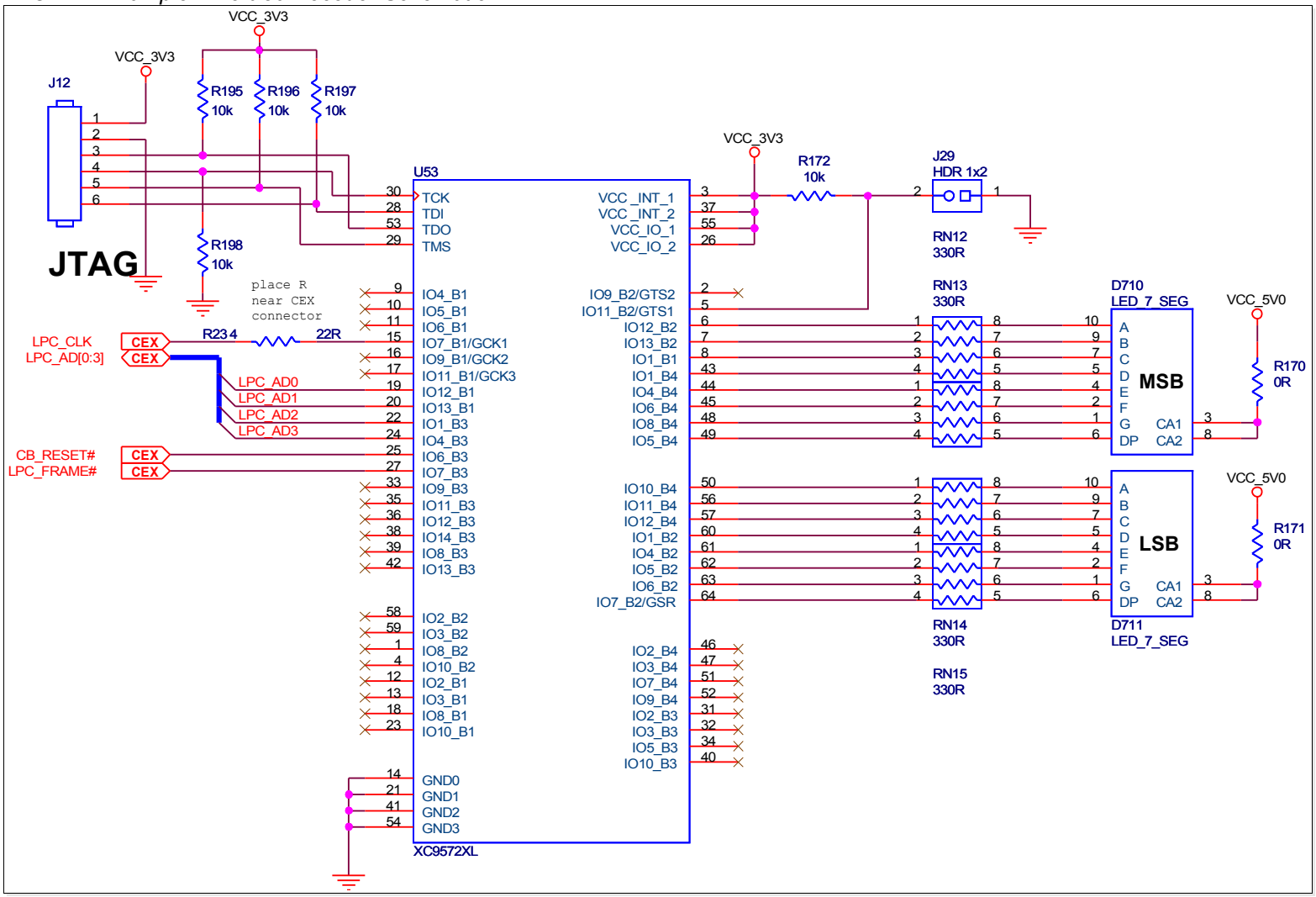
FWH pin 29 configures the FWH into one of two modes: if high, the FWH is in the Programmer configuration. If low, it is in the firmware hub configuration. For normal operation on a Carrier Board, this pin should be tied low.

FWH pin 31 is the clock input. The clock source is the LPC_CLK signal from the COM Express Module.

FWH pin 2 – RST# supports Chip Reset. The LPC_RESET# signal from the COM Express Module drives the reset. The pin functions the same as INIT# above.

2.15.2.4. LPC PLD Example – Port 80 Decoder

Figure 39: LPC PLD Example – Port 80 Decoder Schematic



The following applies to Figure 39 above.

The JTAG header may be used to program the PLD in-circuit.

The LPC bus is the interface to the Module host system.

Two seven-segment LED displays show the Port 80 POST (Power On Self Test) codes.

PLD outputs drive the LEDs.

On some systems, a BIOS setting is needed to allow POST codes to be forwarded to the LPC bus.

2.15.2.5. SuperIO

Figure 40: LPC Super I/O Example

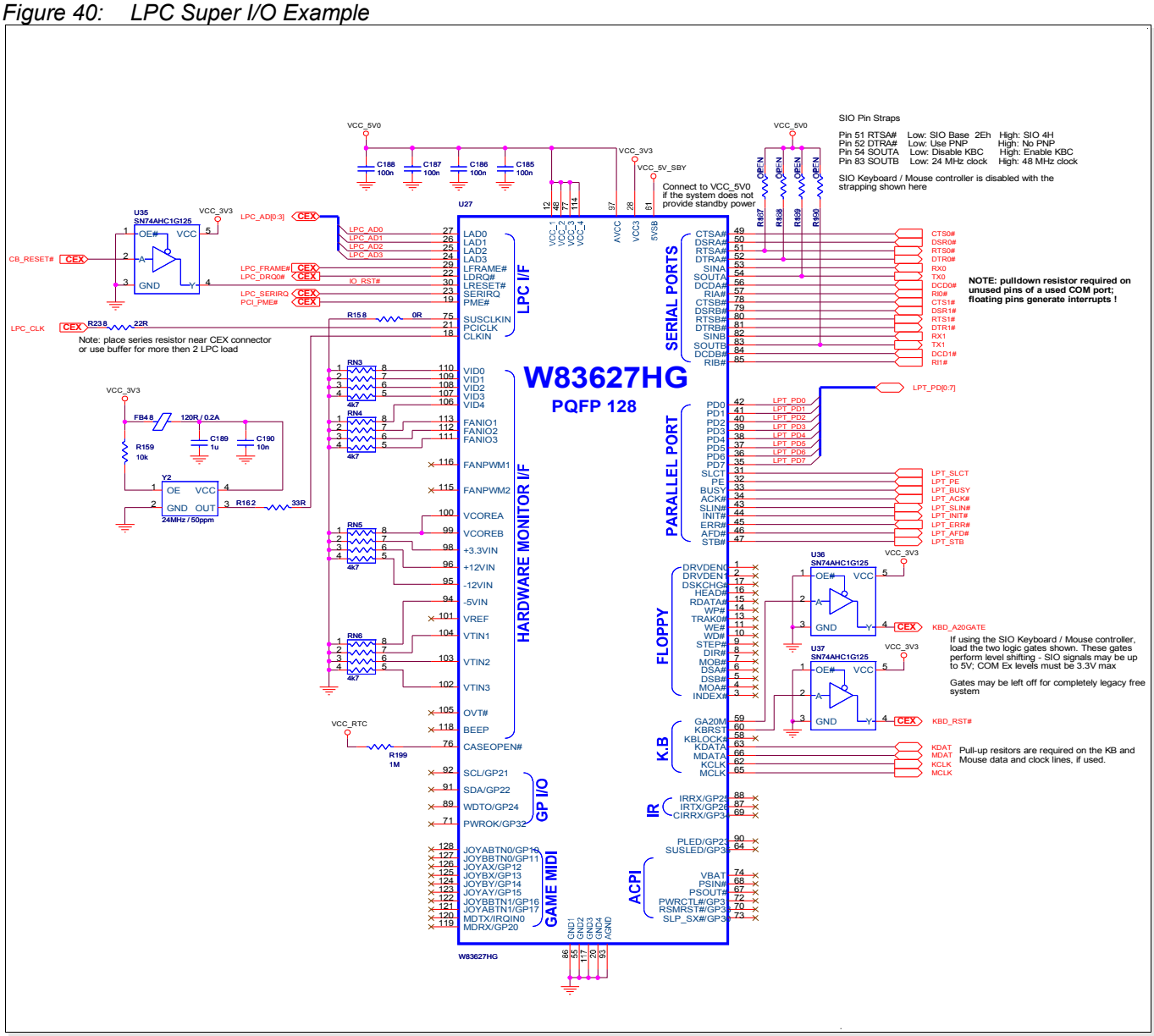
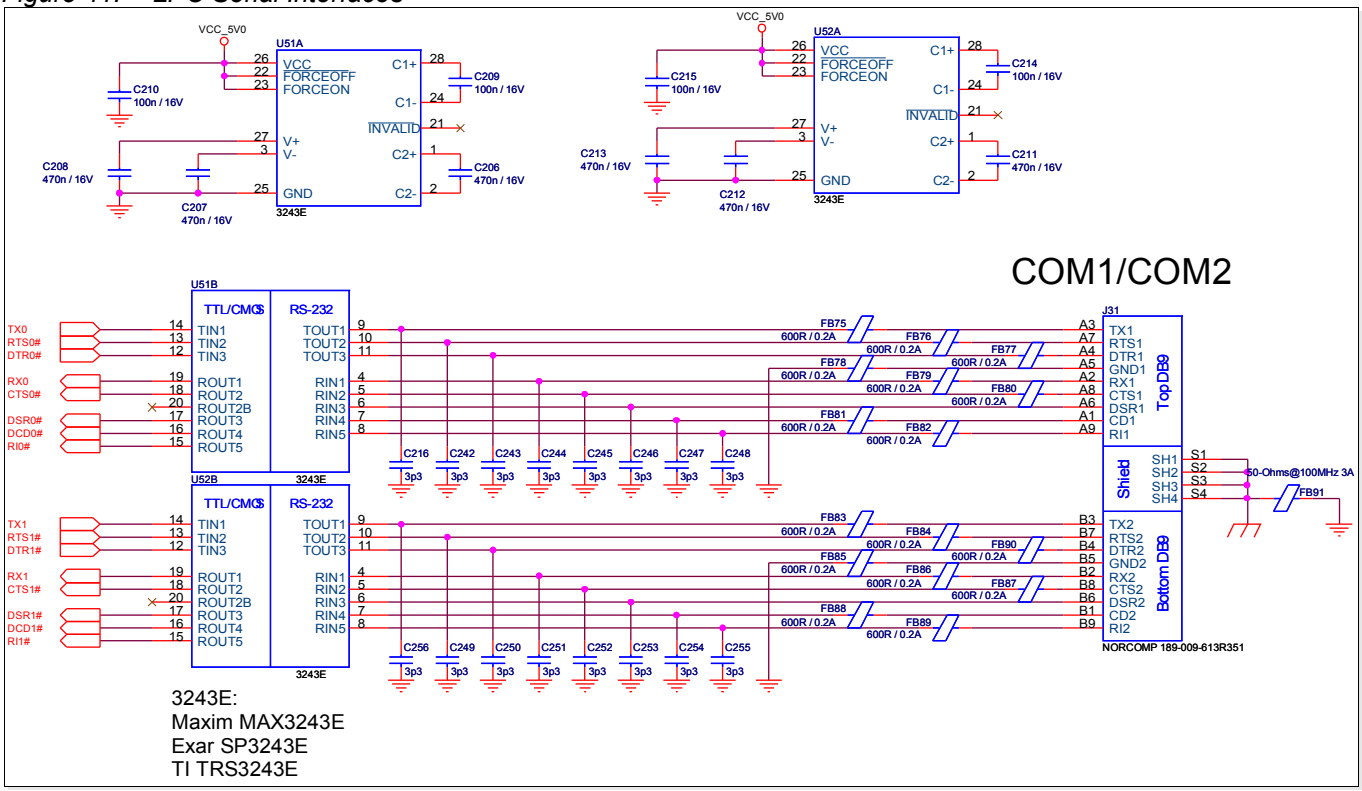


Figure 41: LPC Serial Interfaces



Note: ***Connection between logic GND and chassis depends on grounding architecture. Connect GND with chassis at a single point even though this connection is drawn on all schematic examples throughout this document.***

2.15.3. Routing Considerations

2.15.3.1. General Signals

LPC signals are similar to PCI signals and may be treated similarly. Route the LPC bus as 55 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching is not required.

See Section 6.5.3 'LPC Trace Routing Guidelines' on page 142 below.

2.15.3.2. Bus Clock Routing

The LPC bus clock is similar to the PCI bus clock and should be treated similarly. The COM Express Specification allows 1.6 ns +/- 0.1ns for the propagation delay of the LPC clock from the Module pin to the LPC device destination pin. Using a typical propagation delay value of 180 ps / inch, this works out to 8.88 inches of Carrier Board trace for a device-down application. For device-up situations, 2.5 inches of clock trace are assumed to be on the LPC slot card (by analogy to the PCI specification). This is deducted from the 8.88 inches, yielding 6.38 inches.

On a Carrier Board with a small form factor, serpentine clock traces may be required to meet the clock-length requirement.

Route the LPC clock as a single-ended, 55 Ω trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground referenced internal layer is preferred to reduce EMI.

The COM Express Specification brings a single LPC clock out of the Module. If there are multiple LPC targets on the Carrier Board design, then a zero delay clock buffer is recommended. The buffer recommendation is the same as the one shown for the PCI clock in Section 2.3.5.1 'Reference Clock Buffer' on page 21 above. This provides a separate copy of the LPC clock to each target. The overall delay from the Module LPC clock pin to the target LPC device clock pin should be 1.6 ns.

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the COM Express specification and the 'PCI Local Bus Specification Revision 2.3'. In addition to this refer to Section 6.5.1 'PCI Trace Routing Guidelines' on page 140 below.

2.16. General Purpose I2C Bus Interface

The I2C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (up to 400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers. The COM Express Specification defines five I2C interfaces that are brought to the Module connector for use on the Carrier. Three of these interfaces are for very specific functions (VGA, LVDS, and DVO), the fourth interface is the SMBus used primarily for management and the fifth interface is a general purpose I2C interface. The General Purpose I2C Interface is also used to support a Carrier based ROM that contains Carrier PCIe mapping information for the BIOS. Not all COM Express Modules support that feature.

The lack of a common software interface for the General Purpose I2C interface might limit vendor interoperability. Carriers that use this interface will need to contact Module vendors for further information.

2.16.1. Signal Definitions

The general purpose I2C Interface is powered from 3.3V. The I2C_DAT is an open collector line with a pull-up resistor located on the Module. The I2C_CK has a pull-up resistor located on the Module. The Carrier should not contain pull-up resistors on the I2C_DAT and I2C_CK signals. Carrier based devices should be powered from 3.3V. The use of Early Power for a Carrier I2C device will require a bus isolator to prevent leakage to other I2C devices on 3.3V power.

At this time, there is no allocation of I2C addresses between the Module and Carrier. Carrier designers will need to consult with Module providers for address ranges that can be used on the Carrier.

A reference to the I2C source specification can be found in Section 8 'Applicable Documents and Standards' on page 148.

The COM Express general purpose I2C pins are on the B row of the COM Express A-B connector as shown in Table 31 below.

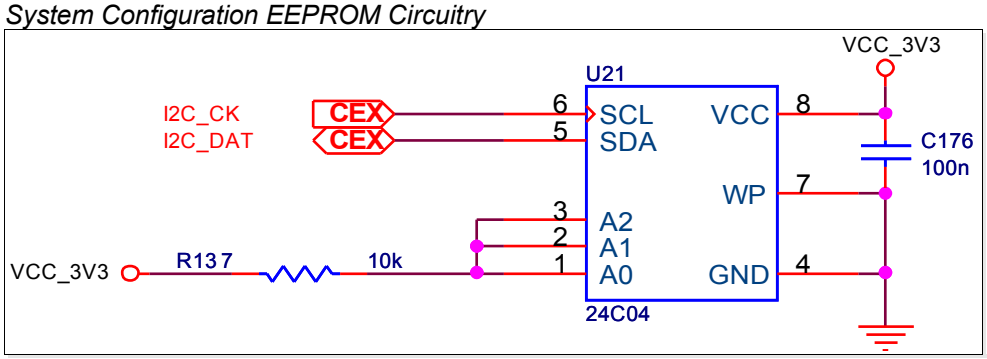
Table 30: General Purpose I2C Interface Signal Descriptions

Signal	Pin	Description	I/O	Pwr Rail	Comment
I2C_CK	B33	General Purpose I2C Clock output	O CMOS	3.3V	
I2C_DAT	B34	General Purpose I2C data I/O line.	I/O OD CMOS	3.3V	

2.16.2. Reference Schematics

The COM Express specification recommends implementing a serial I2C EEPROM of at least 2kbit on the Carrier Board where all the necessary system configuration can be saved. For more information about the content of this system configuration EEPROM, refer to the COM Express Specification. The circuitry in Figure 42 below shows how to connect an Atmel 'AT24C04' 4kbit EEPROM to the General Purpose I2C bus on the COM Express Carrier Board (http://www.atmel.com). According to the COM Express specification, the I2C address lines A2, A1 and A0 of the system configuration EEPROM must be pulled high. Depending on the EEPROM size this leads to the I2C addresses 1010 111x (2kbit), 1010 110x (4kbit), or 1010 100x (8kbit).

Figure 42: System Configuration EEPROM Circuitry



The EEPROM stores configuration information for the system of the Carrier Board. The data structure used is defined in the COM Express Specification. The Specification recommends but does not require the use of this system configuration EEPROM. The Module BIOS may check the Carrier Board configuration EEPROM but is not required to do so by the Specification.

The Atmel AT24C04 with 4Kb organized as 512 x 8 is a suitable device in an 8-pin SOIC package. For applications that require additional ROM or memory capacity such as 8Kb (1K x 8) or 16Kb (2K x 8), an Atmel AT24C08A may be used.

The COM Express Specification requires a minimum capacity of 2Kb. The Atmel AT24C02 meets this minimum capacity.

Address inputs A0, A1, A2 are pulled high. This creates the I2C address 1010 111x, which is required by the COM Express Specification. EEPROM devices internally set I2C address lines A6, A5, A4, A3 to binary value 1010.

WP (write protect) is pulled low for normal read/write.

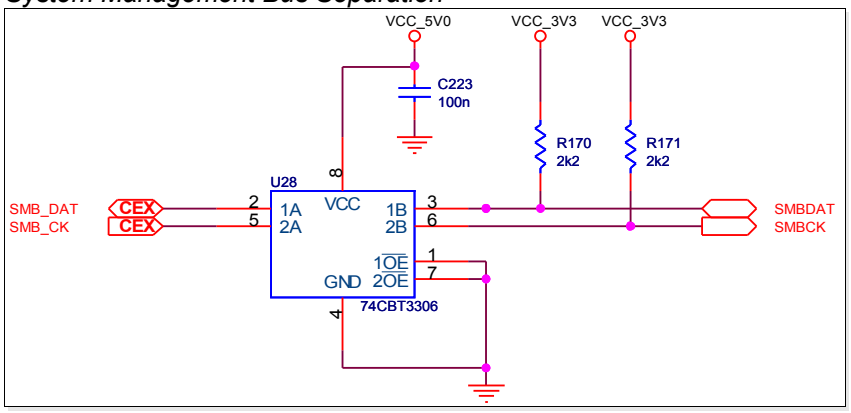
2.16.3. Routing Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by your Module vendor. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 12pF of capacitance, and a PWB trace has 3.8pF per inch of trace length. Do not connect Standby Power to I2C devices unless bus isolation is used to prevent back feeding of voltage from the Suspend supply to the Non-Suspend supply voltages.

2.17. System Management Bus (SMBus)

The SMBus is primarily used as an interface to manage peripherals such as serial presence detect (SPD) on RAM, thermal sensors, PCI/PCIe devices, smart battery, etc. The devices that can connect to the SMBus can be located on the Module and Carrier. Designers need to take note of several implementation issues to ensure reliable SMBus interface operation. The SMBus is similar to I2C. I2C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition. Designers are urged to use SMBus devices when possible over standard I2C devices. COM Express Modules are required to power SMBus devices from Early Power in order to have control during system states S0-S5. The devices on the Carrier Board using the SMBus are normally powered by the 3.3V main power. To avoid current leakage between the main power of the Carrier Board and the Suspend power of the Module, the SMBus on the Carrier Board must be separated by a bus switch from the SMBus of the Module. Figure 43 below shows an appropriate bus switch circuit for separating the SMBus of the Carrier Board from the SMBus of the Module. However, if the Carrier Board also uses Suspend powered SMBus devices that are designed to operate during system states S3-S5, then these devices must be connected to the Suspend powered side of the SMBus, i. e. between the COM Express Module and the bus switch. Since the SMBus is used by the Module and Carrier, care must be taken to ensure that Carrier based devices do not overlap the address space of Module based devices. Typical Module located SMBus devices and their addresses include memory SPD (serial presence detect 1010 000x, 1010 001x), programmable clock synthesizes (1101 001x), clock buffers (1101 110x), thermal sensors (1001 000x), and management controllers (vendor defined address). Contact your Module vendor for information on the SMBus addresses used.

Figure 43: System Management Bus Separation



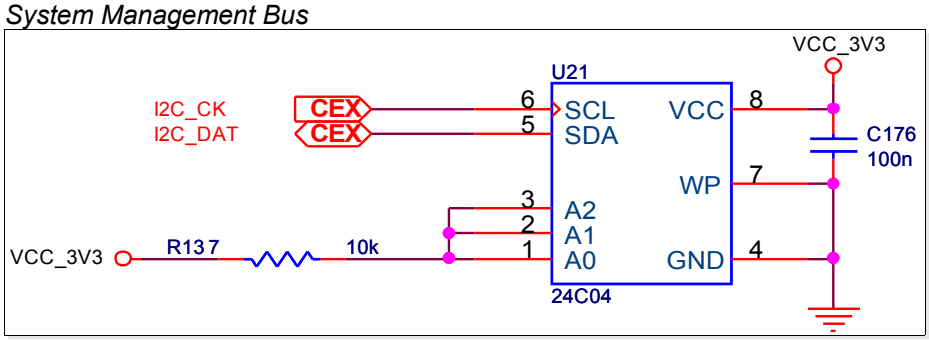
2.17.1. Signal Definitions

Table 31: System Management Bus Signals

Signal	Pin	Description	I/O	Pwr Rail	Comment
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD CMOS	3.3V Suspend rail	
SMB_DAT	B14	System Management bidirectional data line.	I/O OD CMOS	3.3V Suspend rail	
SMB_ALERT#	B15	System Management Bus Alert	I CMOS	3.3V Suspend Rail	

2.17.2. Reference Schematics

Figure 44: System Management Bus



2.17.3. Routing Considerations

SMBus should be connected to all or none of the PCIe/PCI devices and slots. A general recommendation is to not connect these devices to the SMBus.

The maximum load of SMBus lines is limited to 3 external devices. Please contact your module vendor if more devices are required.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

Contact your Module vendor for a list of SMBus addresses used on the Module. Do not use the same address for Carrier located devices.

2.18. Miscellaneous Signals

Table 32: Miscellaneous Signals

Signal	Pin	Description	I/O	Comment
Type0# Type1# Type2#	C54 C57 D57	The Type pins indicate the COM Express pinout type of the Module. To indicate the Module's pinout type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pinout type is detected.	O 5V PDS	
SPKR	B32	Output used to control an external FET or a logic gate to drive an external PC speaker.	O 3.3V CMOS	
BIOS_DISABLE#	A34	Input to disable the Modules BIOS flash memory chip. This signal provides the ability to implement an external BIOS flash memory chip that can be located on the Carrier Board.	I 3.3V CMOS	See Section 2.15.2.3 'LPC Firmware Hub' on page 92 above
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V CMOS	
KBD_RST#	A86	Input signal of the Module used by an external keyboard controller to force a system reset.	I 3.3V CMOS	
KBD_A20GATE	A87	Input signal of the Module used by an external keyboard controller to control the CPU A20 gate line. The A20 gate restricts the memory access to the bottom megabyte of the system. Pulled high on the Module.	I 3.3V CMOS	
GPO0 GPO1 GPO2 GPO3	A93 B54 B57 B63	General Purpose Outputs for system specific usage.	O 3.3V CMOS	Refer to the Module's users guide for information about the functionality of these signals.
GPI0 GPI1 GPI2 GPI3	A54 A63 A67 A85	General Purpose Input for system specific usage. The signals are pulled up by the Module.	I 3.3V CMOS	Refer to the Module's users guide for information about the functionality of these signals.

2.18.1. Module Type Detection

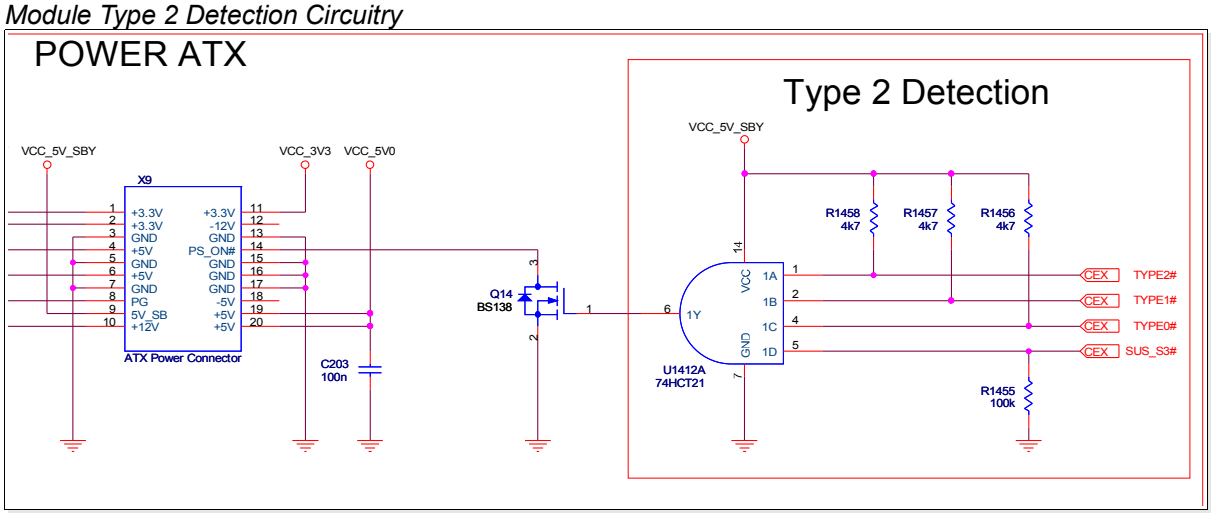
The COM Express Specification includes three signals to determine the pinout type of the Module connected to the Carrier Board. If an incompatible Module pinout type is detected, external logic should prevent the Carrier Board from powering up the whole system by controlling the 12V supply voltage. The pins 'TYPE0#', 'TYPE1#' and 'TYPE2#' are either left open (NC) or strapped to ground (GND) by the Module to encode the pinout type according to the following table. The Module Type 1 has no encoding. For more information about this subject, refer to the COM Express Specification.

Table 33: Module Type Detection

Module Type	Pin TYPE0#	Pin TYPE1#	Pin TYPE2#	
Module Type 1	X (don't care)	X (don't care)	X (don't care)	
Module Type 2	NC	NC	NC	
Module Type 3	NC	NC	GND	No IDE interface
Module Type 4	NC	GND	NC	No PCI interface
Module Type 5	NC	GND	GND	No IDE, no PCI interface

Figure 45 below illustrates a detection circuitry for Type 2 Modules. If any Module type other than Type 2 is connected, the 'PS_ON#' signal, which controls the ATX power supply, is not driven low by the Module, and hence the main power rails of the ATX supply do not come up. The Type Detection pins of the Module must be pulled up on the Carrier Board to the 5V Suspend voltage rail.

Figure 45: Module Type 2 Detection Circuitry



2.18.2. Speaker Output

The PC-AT architecture provides a speaker signal that creates beeps and chirps. The signal is a digital-logic signal that is created from system timers within the core chipset. The speaker provides feedback to the user that an error has occurred. The system BIOS usually drives the speaker line with a set of beep codes to indicate hardware problems such as a memory test failure, a missing video device, or a missing keyboard. Application software often uses the PC-AT speaker to flag an error such as an invalid key press.

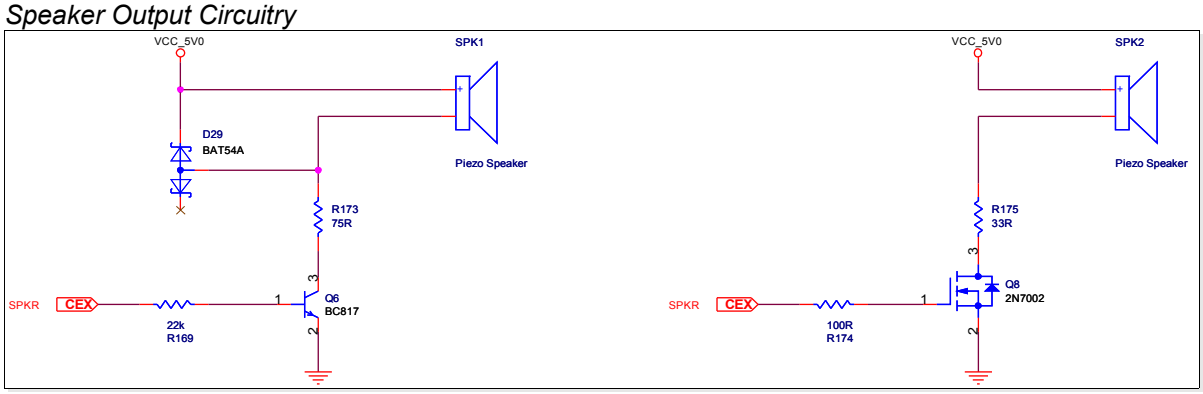
This speaker signal should not be confused with the analog-audio signals produced by the audio CODEC. In many systems, the PC-AT speaker signal is fed into one of the audio CODEC inputs, allowing it to be mixed with other audio signals and heard on the audio transducer (speakers and headphones) that the CODEC drives.

The COM Express Module provides a speaker output signal called 'SPKR', which is intended to drive an external FET or a logic gate to connect a PC speaker.

The 'SPKR' signal is often used as a configuration strap for the Modules chipset. It should not be connected to a pull-up or pull-down resistor, which could overwrite the internal chipset configuration and result in a malfunction of the Module.

The PC-AT audio transducer that is used for error messages is usually a small, low-cost loudspeaker or piezoelectric-electric buzzer. A buffering between the Module SPKR pin and the audio transducer is required. An example circuit is shown in Figure 46 below. The net SPKR is sourced from Module pin B32. If the transducer is a low impedance device, such as an 8 Ω speaker, then a larger resistor value and package size for R173/R175 is in order.

Figure 46: Speaker Output Circuitry



2.18.3. RTC Battery Implementation

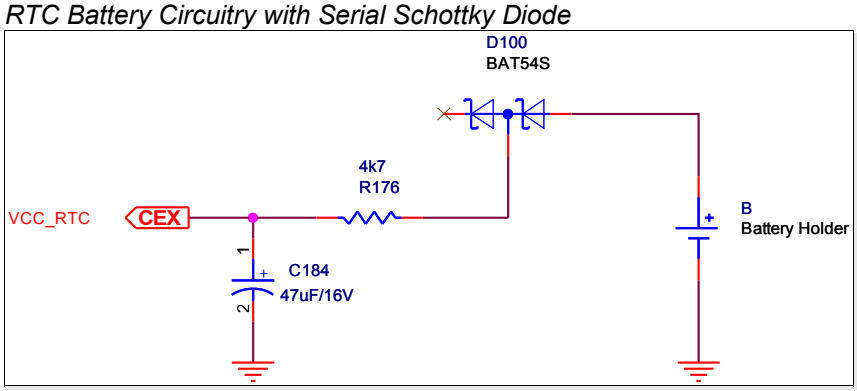
The Real Time Clock (RTC) is responsible for maintaining the time and date even when the COM Express Module is not connected to a main power supply. Usually a +3V lithium battery cell is used to supply the internal RTC of the Module. The COM Express Specification defines an extra power pin 'VCC_RTC', which connects the RTC of the Module to the external battery. The specified input voltage range of the battery is defined between +2.0V and +3.0V. The signal 'VCC_RTC' can be found on the Module's connector row A pin A47.

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series Schottky diode or a series resistor. There are two implementation possibilities and the following examples explain the advantages and disadvantages of each one.

The safest way to implement a RTC battery circuitry is by using a Schottky diode as shown in Figure 47 below. This method offers protection against a possible explosion hazard as a result of reverse current flowing to the battery. Moreover, this implementation offers more flexibility when choosing battery type and manufacturer. Lithium batteries are the most common form of battery used in this scenario.

A big drawback of this circuitry is that the battery voltage monitoring result displayed by the COM Express Module will be inaccurate due to current leakage on the Module side. When the system is running, this current leakage loads the capacitor of the battery circuitry. This leads to a higher voltage on the signal pin 'VCC_RTC' and therefore produces inaccurate monitoring results.

Figure 47: RTC Battery Circuitry with Serial Schottky Diode



2.18.3.1. RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the Carrier Board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current, it should be measured when the complete system is disconnected from AC power.

For information about the power consumption of the RTC circuit, refer to the Module's user's guide.

2.18.4. Power Management Signals

COM Express specifies a set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states from S0 to S5. The minimum hardware requirements for an ACPI compliant system are an ATX conforming power supply and a power button.

The following table provides a short description of the ACPI defined system states S0 to S5 including the corresponding power rail state. For more information about ACPI and the several system power states, refer to the 'Advanced Configuration and Power Interface Specification Revision 3.0'.

Table 34: System States S0-S5 Definitions

System State	Description	Power Rail State
S0 Full On	All components are powered and the system is fully functional.	Full power on all power rails.
S1 Power-on Standby (POS)	In sleeping state, no system context is lost, hardware maintains all system context. During S1 operation some system components are set into low power state.	Full power on all power rails.
S2	Not supported.	
S3 Suspend to RAM (STR)	The current system state and context is stored in main memory and all unnecessary system logic is turned off.	Only main memory and logic required to wake-up the system remain powered by the Suspend voltages. All other power rails are switched off.
S4 Suspend to Disk (STD) Hibernate	The current system state and context is stored on disk and all unnecessary system logic is turned off. S4 is similar to S5 and just supported by OS.	Similar to S5; All other power rails are switched off.
S5 Soft Off	In S5 state the system is switched off. Restart is only possible with the power button or by a system wake-up event such as 'Wake On LAN' or RTC alarm.	Suspend power rails are powered. All other power rails are switched off.

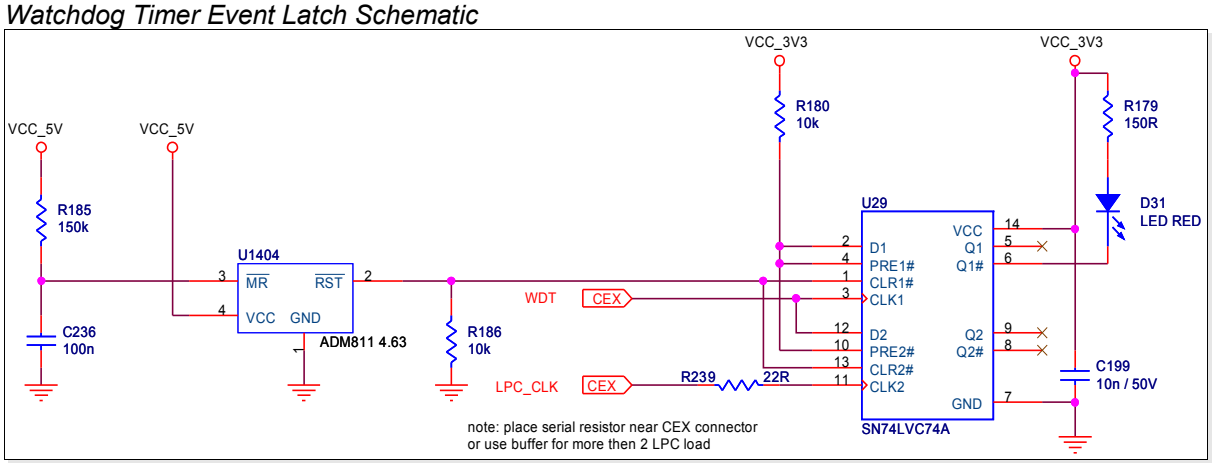
Table 35: Power Management Signal Descriptions

Signal	Pin	Description	I/O	Comment
PWRBTN#	B12	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.	I 3.3V Suspend CMOS	Drive with >=10mA
SYS_RESET#	B49	Reset input signal. This signal may be driven to low by external circuitry such as a reset button to hold the system Module in hardware reset.	I 3.3V Suspend CMOS	Drive with >=10mA
CB_RESET#	B50	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board.	O 3.3V Suspend CMOS	
PWR_OK	B24	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation.	I 3.3V CMOS	
SUS_STAT#	B18	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode.	O 3.3V Suspend CMOS	
SUS_S3#	A15	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).	O 3.3V Suspend CMOS	This signal can be used to control the ATX power supply via the *'PS_ON#'* signal.
SUS_S4#	A18	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk).	O 3.3V Suspend CMOS	

Signal	Pin	Description	I/O	Comment
SUS_S5#	A24	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).	O 3.3V Suspend CMOS	
WAKE0#	B66	PCI Express wake-up event signal.	I 3.3V Suspend CMOS	
WAKE1#	B67	General purpose wake-up signal.	I 3.3V Suspend CMOS	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.	I 3.3V Suspend CMOS	

2.18.5. Watchdog Timer

Figure 48: Watchdog Timer Event Latch Schematic



The Watchdog Timer (WDT) event signal is provided by the COM Express Module. The WDT output is active-high. It is sourced from Module pin B27.

The WDT event can cause the system to reset by making appropriate Carrier Board connections. It also may be possible to configure the Module to reset on a WDT event; check the manufacturer's Module Users Guide.

If the WDT output is used to cause a system reset, the WDT output will be cleared by the system reset event.

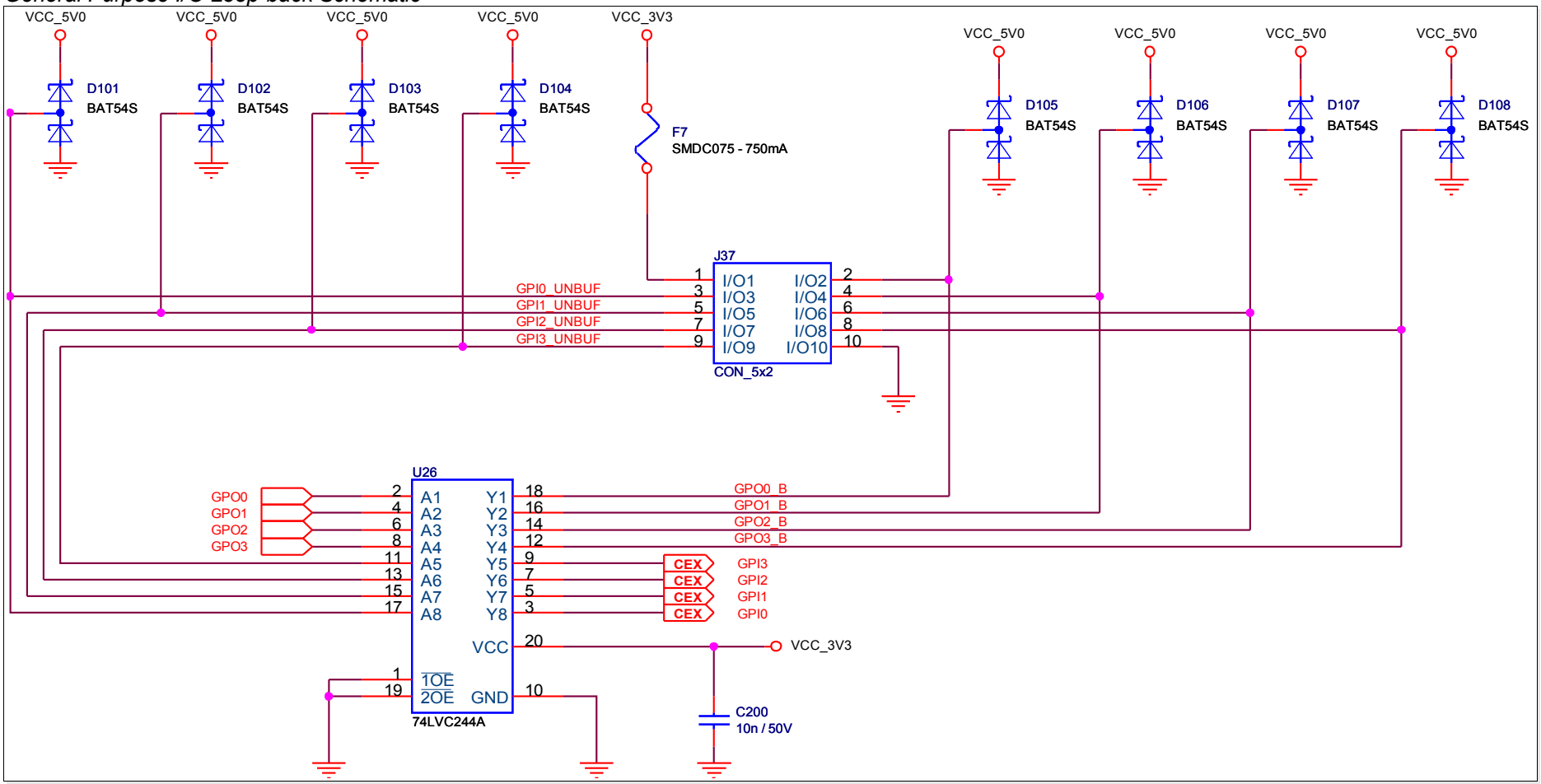
The WDT can be latched to drive a LED for a visual indication of an event, as shown in this example. Note that the latch is powered by a power rail that is active in all power states, including the soft-off state. The latch is only cleared by a complete power cycle. The cold power-up cycle is signaled by the RSMRST# net (Resume Reset, active low). A Carrier Board reset monitor, not shown in this figure, is required to generate the RSMRST# signal. The reset monitor should monitor the 5V or 3.3V Suspend power rail (V5.0_S5 or V3.3_S5).

2.18.6. General Purpose Input/Output (GPIO)

Table 36: GPIO Signal Definition

Signal	Pin	Description	I/O	Comment
GPI0	A54	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI1	A63	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI2	A67	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPI3	A85	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS	
GPO0	A93	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO1	B54	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO2	B57	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	
GPO3	B63	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS	

Figure 49: General Purpose I/O Loop-back Schematic



There are 4 GPI (General Purpose Inputs) and 4 GPO (General Purpose Outputs) pins in Figure 49 above.

The signals drive switch inputs such as Lamps, Relays, and Sensors.

GPI signals from a header are shown with protection diodes. The signals are connected for input to the COM Express Module.

GPO signals from the COM Express Module are shown buffered. The signals are connected to the header with protection diodes.

2.18.7. Thermal Interface

COM Express provides the 'THRM#' and 'THRMTRIP#' signals, which are used for system thermal management. In most current system platforms, thermal management is closely associated with system power management. For more detailed information about the thermal management capabilities of the COM Express Module, refer to the manufacturer's Module's user's guide.

Table 37: Thermal Management Signal Descriptions

Signal	Pin	Description	I/O	Comment
THRM#	B35	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V CMOS	
THRMTRIP#	A35	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V CMOS	

3. Power and Reset

3.1. General Power requirements

COM Express calls for the Module to be powered by a single 12V power rail, with a +/-5% tolerance. Some vendors offer a wider input range on this rail. COM Express Modules may consume significant amounts of power – 25 to 50W is common, and higher levels are allowed by the standard. Close attention must be paid by the Carrier Board designer to ensure adequate power delivery. Details are given in the sections below.

If Suspend functions such as Suspend-to-RAM, Suspend-to-disk, wake on power button press, wake on USB activity, etc. are to be supported, then a 5V Suspend power source must also be provided to the Module. If Suspend functions are not used, the Module VCC_5V_SBY pins should be left open. On some Modules, there may be a slight power efficiency advantage to connecting the Module VCC_5V_SBY rail to VCC_5V rather than leaving the Module pin open. Please contact your module vendor for further details.

Carrier Boards typically require other power rails such as 5V, 3.3V, 3.3V Suspend, etc. These may be derived on the Carrier Board from the 12V and 5V Suspend rails.

3.1.1. VCC_12V Rise Time Caution and Inrush Currents

Direct connection of a COM Express Module to a low impedance supply such as a battery pack may result in excessive inrush currents. The supply to the COM Express Module should be slew limited to limit the input voltage ramp rate. A typical ATX supply ramps at about 2.5 volts per millisecond.

3.2. ATX and AT Style Power Control

3.2.1. ATX vs AT Supplies

ATX power supplies are in common use in contemporary PCs. ATX supplies have two sets of power rails: a set for normal operation (12V, 5V, 3.3V and -12V) and a separate 5V Suspend rail. The 5V Suspend rail is present whenever the ATX supply has AC input power. The other rails are on only when a control signal from the PC hardware known as PS_ON# is held low by the motherboard, allowing software control of the power supply. The PC motherboard may implement several mechanisms for controlling the AC power, including a push button switch that switches a low voltage logic signal rather than the AC main power. Other options may be implemented, including the capability to turn on the main power on events such as a keyboard press, mouse activity, etc.

AT power supplies do not have a Suspend rail and do not allow software control of the power supply. An AT supply is on when the supply is connected to the AC main and the power switch that is in series with the AC main input is on. AT supplies are extinct in the commercial PC market, but the term lives on as a reference to a power supply that does not allow software control.

An ATX supply may be converted to AT style operation by simply holding the ATX PS_ON# input low all the time.

3.2.2. Power States

Power states are described by the following terms:

Table 38: Power States

State	Description	Comment
G3	Mechanical Off	AC power to system is removed by a mechanical switch. System power consumption is near zero – the only power consumption is that of the RTC circuits, which are powered by a backup battery.
S5	Soft Off	System is off except for a small subset that is powered by the 5V Suspend rail. There is no system context preserved. VCC_5V_SBY current consumption is system dependent, and it may be from tens of milliamps up to several hundred milliamps.
S4	Suspend to Disk	System is off except for a small subset that is powered by the 5V Suspend rail. System context is preserved on a non-volatile disk media (that is powered off). VCC_5V_SBY current consumption is system dependent, and it may be from tens of milliamps up to several hundred milliamps.
S3	Suspend to RAM	System is off except for system subset that includes the RAM. Suspend power is provided by the 5V Suspend rail. System context is preserved in the RAM. VCC_5V_SBY current consumption is system dependent, and it may be from several hundred milliamps up to a maximum of 2A.
S0	On	System is on.

COM Express signals SUS_S5#, SUS_S4# and SUS_S3# have the following behavior in the Power States:

Table 39: Power State Behavior

State	SUS_S5#	SUS_S4#	SUS_S3#
G3	NA	NA	NA
S5	Low	Low	Low
S4	High	Low	Low
S3	High	High	Low
S0	High	High	High

3.2.3. ATX and AT Power Sequencing Diagrams

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 50 below.

A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 51 below below.

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details.

Figure 50: ATX Style Boot – Controlled by Power Button

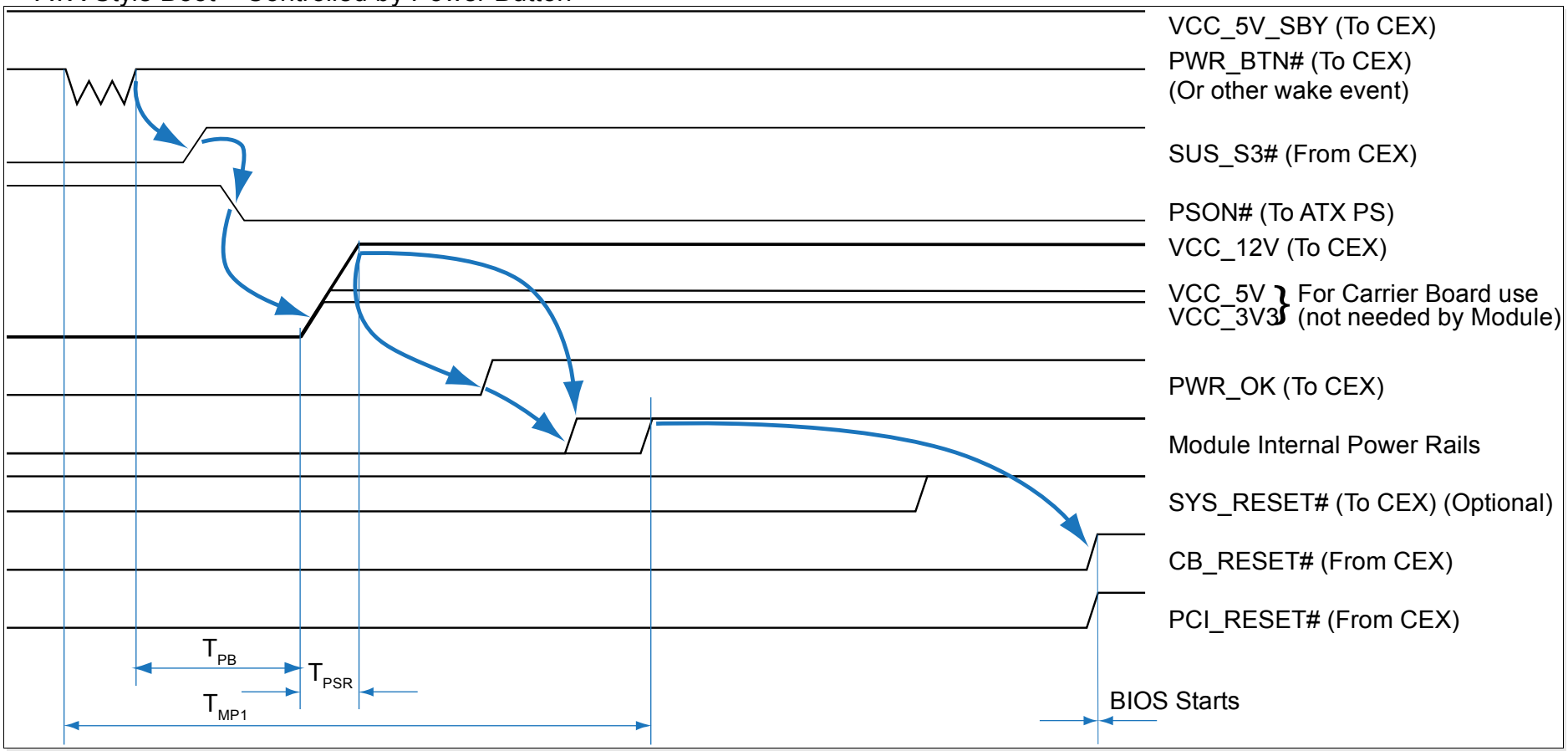


Figure 51: AT Style Power Up Boot

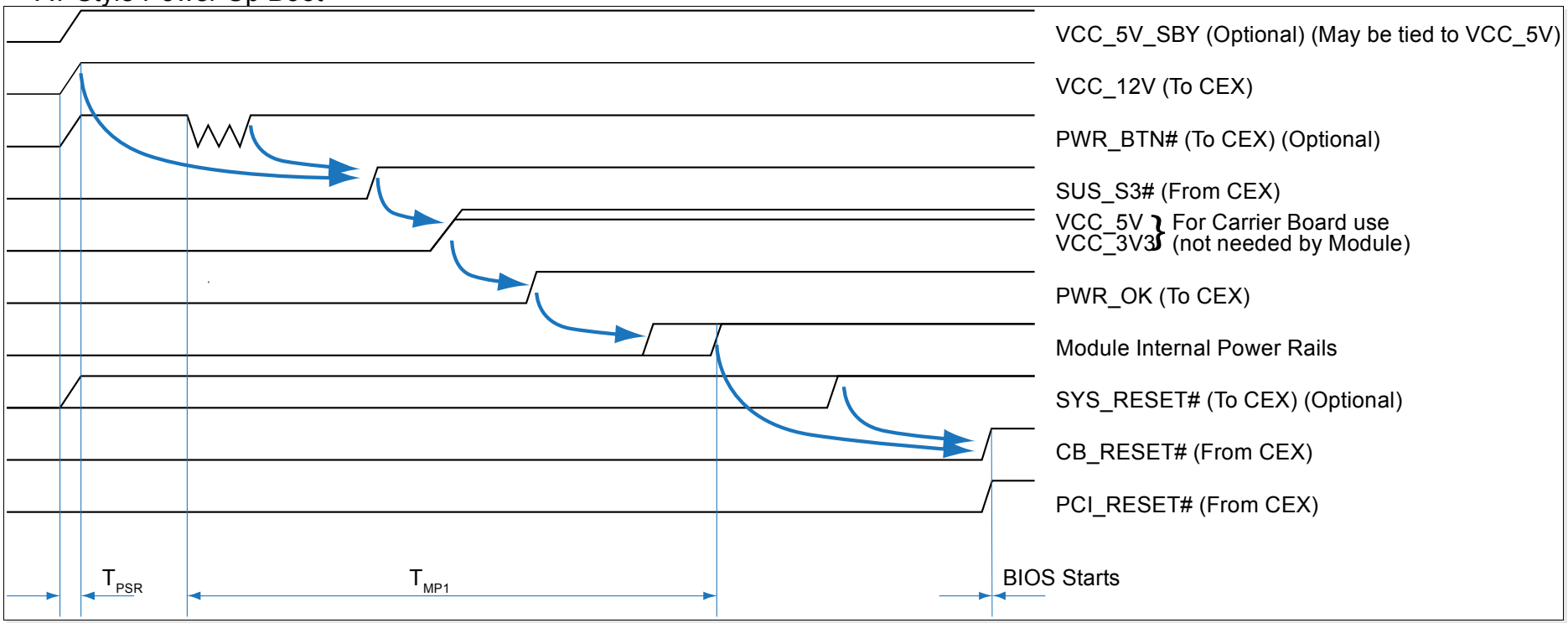


Table 40 below below indicates roughly what time ranges can be expected during the boot process, per Figure 50 and Figure 50 above. Check with your Module vendor if more specific information is required.

Table 40: ATX and AT Power Up Timing Values

Parameter	Min Value	Max Value	Description	Comments
TPB	10ms	500ms	Push Button Power Switch – time to bring Module chipset out of Suspend mode	Applies only to ATX Style Power Up
TPSR	0.1ms	20ms	Power Supply Rise Time	

Notes

There is a period of time (TMP1 in Figure 50 and Figure 51 above) during which the Carrier Board circuits have power but the COM Express Module main internal power rails are not up. This is because almost all COM Express internal rails are derived from the external VCC_12V and there is a non-zero start-up time for the Module internal power supplies.

Carrier Board circuits should not drive any COM Express lines during the TMP1 interval except for those identified in the COM Express Specification as being powered from a Suspend power rail. Almost all such signals are active low. Such signals, if used, should be driven low by open drain Carrier Board circuits to assert them. Pull-ups, if present, should be high value (10K to 100K) and tied to VCC_5V_SBY.

The line PWR_OK may be used during the TMP1 interval to hold off a COM Express Module boot. Sometimes this is done, for example, to allow a Carrier Board device such as an FPGA to be configured before the Module boots.

The deployment of Carrier Board pull-ups on COM Express signals should be kept to a minimum in order to avoid back-driving the COM Express signal pins during this interval. Carrier Board pull-ups on COM Express signal pins are generally not necessary – most signals are pulled up if necessary on the Module.

3.2.4. Power Monitoring Circuit Discussion

Contemporary chipsets used in COM Express Modules incorporate a state machine or micro-controller that is powered from a Suspend power rail (i.e. a power rail that is derived from VCC_5V_SBY and is on whenever the ATX power supply has incoming AC line power). This state machine or micro-controller operates autonomously from the main CPU on the Module. The function of this state machine or micro-controller is to manage the system power states. It monitors various inputs (e.g. PWRBTN#, WAKE0#, WAKE1#, etc.) that can cause power state changes, and outputs status signals (e.g. SUS_S5#, SUS_S4#, SUS_S3#, SUSPEND#) that can be used by system hardware to control various power supplies and power planes in the system.

3.2.5. Power Button

The COM Express PWRBTN# input may be used by Carrier Board hardware to implement ATX style power control. A schematic example of how to do this is given in 3.3.1 'ATX Power Supply' on page 118 below. The COM Express PWRBTN# input is typically de-bounced by the Module chipset.

The behavior of the system after a power button press depends on the Module chipset capabilities and on the Module vendor's hardware and BIOS implementation. With Modules based on the Intel 915GM, 945GM and 965GM chipsets, the following behaviors may be set by RTC well chipset register settings:

Table 41: Power Button States

State	Description
Always On	No Power Button press needed Chipset de-asserts SUS_S5#, SUS_S4# and SUS_S3# after Suspend rail to chipset is stable
Wait For Power Button Press	Chipset remains in Suspend state until power button press is received
Last State	If unit was “on” when power was removed, then unit returns to “on” state when power is restored

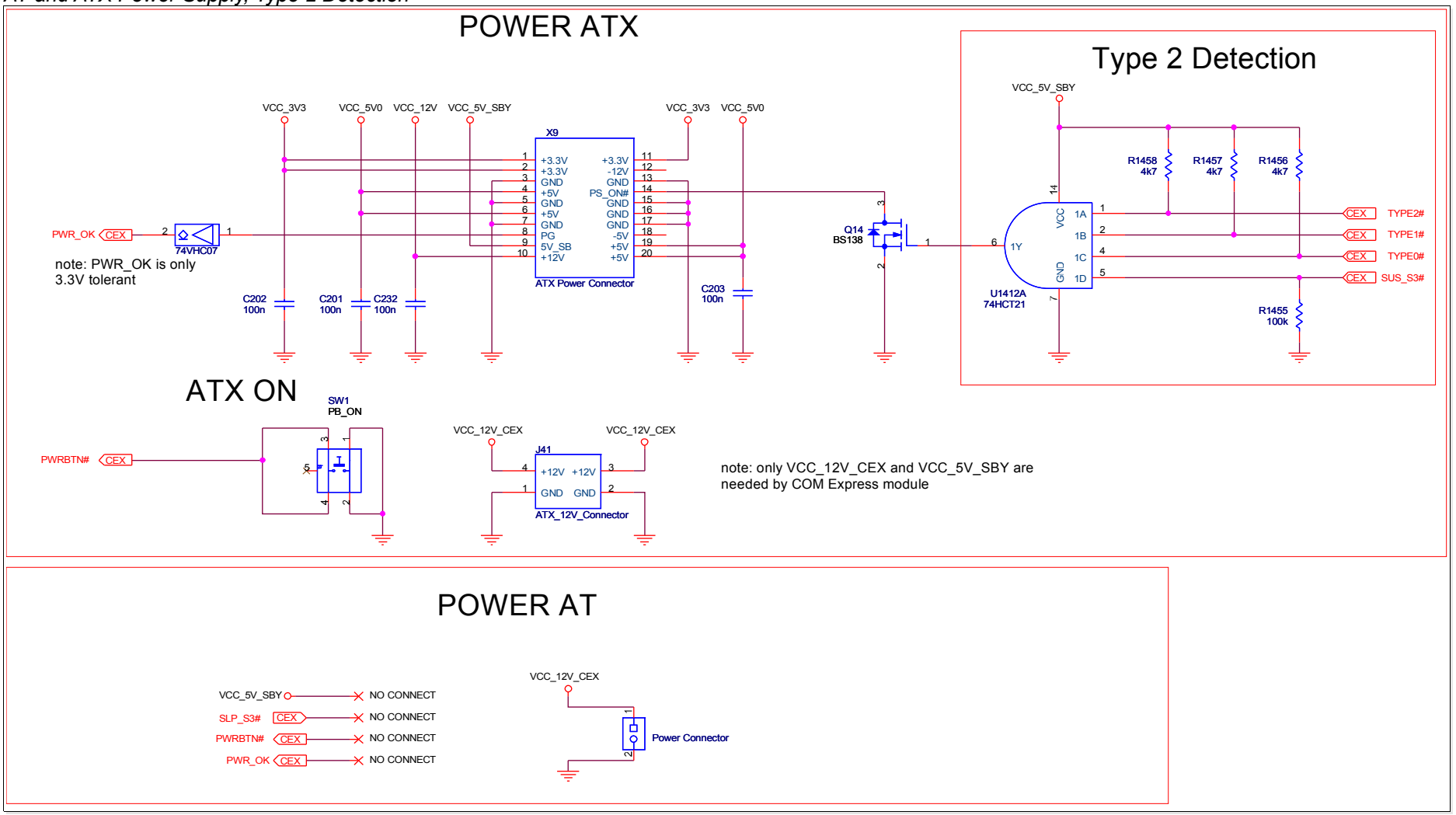
3.3. Reference Schematics

3.3.1. ATX Power Supply

ATX power supplies are used in millions of desktop PCs and are often used in OEM equipment as well. They are inexpensive and are readily available. An ATX power supply provides more power rails (two separate +12V rails, +5V, +3.3V, -12V and +5V Suspend) than are required by a COM Express Module, but often the Carrier Board and other system components make use of the additional rails.

The following figure shows the ATX power Carrier Board circuitry using a 24 pin ATX main power connector. For systems with power-hungry CPUs or Graphics Cards, two additional +12V power pins may be implemented using an auxiliary 4 pin (2x2) +12V/GND power connector.

Figure 52: AT and ATX Power Supply, Type 2 Detection



The PWRBTN# signal is an input to the COM Express Module. Switch de-bouncing is done on the Module. The falling edge of the PWRBTN# signal can initiate a state transition from S5 (soft off) to S0 (full on). It may also cause the reverse transition, to S5, if the unit is in one of the 'on' states.

The ATX supply is controlled by the net PS_ON# in the figure above. The main ATX supply rails are on when PS_ON# is driven low. To turn the supply off, PS_ON# can be floated. This net is usually derived from an inverted copy of the COM Express SUS_S3# signal, logically ANDed with the module detection circuit. The logic used should be powered from the VCC_5V_SBY rail, as shown in Figure 52 above. For example, it may be desirable to cut off the main power rails if there is a system or CPU over-temperature condition.

Table 42: ATX Signal Names

ATX Signal Name	Description
PS_ON#	Active-low, TTL-level input to ATX supply that, when low, enables all power rails. If high or floating, all ATX power rails are disabled except for the +5V Suspend rail.
PWR_OK	Active-high, TTL-level output signal from the ATX supply that indicates that the +12V, +5V, +3.3V and -12V outputs are all present and OK to use.
+12V1DC	+12V power rail for use by all system components except for the CPU, controlled by PS_ON#
+12V2DC	+12V power rail for use by the CPU, controlled by PS_ON#. This power rail appears on a separate 2x2 connector for CPU use only.
+5VDC	+5V power rail, controlled by PS_ON#
+3.3VDC	+3.3V power rail, controlled by PS_ON#
-12VDC	-12V power rail, controlled by PS_ON#
+5VSB	+5V Suspend power rail, present whenever the ATX supply is connected to its AC power input source.
COM	Common return path – usually referred to as “ground” or GND.

ATX signals are summarized in Table 42 above. Note that there are two separate +12V outputs, +12V1DC and +12V2DC. These are independent +12V sources. Each source is limited to 240W maximum output to meet UL safety requirements. The +12V2DC output is intended for CPU use.

Contemporary ATX supplies have two power connectors on the motherboard:

- A 24-pin connector in a 2x12 array that includes all signals in Table 42 above except for +12V2DC.
- A 4-pin connector in a 2x2 array for CPU power that includes +12V2DC and COM only.

Earlier ATX supplies used a 2x10 connector instead of a 2x12. The two connector versions have compatible pin-outs. The 2x10 cable plug may be used with a 2x12 motherboard receptacle as long as pin 1 of the 2x10 cable plug mates with pin 1 of the 2x12 Carrier Board receptacle.

Very early ATX supplies had a single +12V rail, on a 2x10 connector. The 2x2 CPU connector was not present. ATX power supplies are designed for desktop systems, which often have power-hungry CPUs and peripherals. CPUs that require 80W are common. Most Modules use lower-power CPUs, and the ATX supply capacity may be overkill. In particular, two +12V supplies are not necessary for many COM Express Modules.

3.3.1.1. Minimum Loads

ATX supplies may not start up if the loading on the +12V, +5V and +3.3V rails is too light. The ATX12V Power Supply Design Guide shows suggested minimum loads in various configurations but does not specify what the minimum loads are. The minimum loads required may vary with different power supply vendors. Experience has shown that a dummy load on the order of at least 400 mA is required on the +5V line in COM Express Carrier Boards that use little or no +5V and are powered from ATX supplies.

3.4. Routing Considerations

3.4.1. VCC_12V and GND

The primary consideration for the +12V power input (VCC_12V) to the Module is that the trace be wide enough to handle the maximum expected load, with plenty of margin. A power plane may be used for VCC_12V but is not recommended; VCC_12V should not be used as a reference for high-speed signals, such as PCIe, USB, or even PCI, because there may be switching noise present on VCC_12V.

A 40W CPU Module can draw over 3.5A on the VCC_12V pins. Sizing the VCC_12V delivery trace to handle at least twice the expected load is recommended for good design margin. It is best to keep the Carrier Board VCC_12 trace short, wide, and away from other parts of the Carrier Board. See the following section for advice on how to size the trace.

If there are layer transitions in the power delivery path, use redundant “power” vias – vias that are sized with larger holes and pads than default vias.

For the GND return, it is best to use a solid, continuous plane, or multiple planes, using the heaviest possible copper.

It is very important to connect all available power and ground pins available on the COM Express Module to the Carrier Board.

3.4.2. Copper Trace Sizing and Current Capacity

The current capacity of a PCB trace is proportional to the trace’s cross-sectional area – the product of the trace width and thickness. The trace thickness is proportional to the “weight” of copper used. The copper weight is expressed in ounces per square foot in the United States. Usually people will omit the “per square foot” and just use “ounce” to describe the copper. Copper weights of ½ ounce/ 17µm and sometimes 1 ounce/ 35µm are common for inner layer traces. A copper weight of 1 ounce/ 35µm is common for power planes. A copper weight of ½ ounce/ 17µm results in a thickness of approximately 0.7 mil, and 1 ounce/ 35µm copper yields approximately 1.4 mil. Outer layer traces are usually built with ½ ounce/ 17µm copper, but then are “plated up” with additional conductive material, often yielding an effective copper weight of about 1 ounce/ 35µm. The effective weight of outer layer traces may vary with different PCB processes. Check with your PCB vendor, or play it safe and make conservative assumptions.

Consult sources such as the IPC-2221 for charts that relate copper weight, trace width and trace-current capacity at a given temperature rise to the current capability. It is best to assume a conservative trace temperature rise, such as 10° C maximum, when making trace-width decisions. Per the IPC charts, external layer traces can carry significantly more current than internal layer traces, assuming the same base copper weight and the same temperature rise. Approximate current handling capabilities of selected trace widths read off of the IPC-2221 charts are shown in Table 43 below.

Table 43: Approximate Copper Trace Current Capability per IPC-2221 Charts

Trace Type	Max Current with 10°C Temp Rise	Max Current with 20°C Temp Rise
100 mil wide internal trace ½ ounce/ 17µm base copper	1.3 A	1.8 A
200 mil wide internal trace ½ ounce/ 17µm base copper	2.0 A	3.0 A
400 mil wide internal trace ½ ounce/ 17µm base copper	3.5 A	5.0 A
100 mil wide internal trace 1 ounce/ 35µm base copper	2.1 A	3.0 A
200 mil wide internal trace 1 ounce/ 35µm base copper	3.5 A	5.2 A
400 mil wide internal trace 1 ounce/ 35µm base copper	6.0 A	8.0 A
100 mil wide external trace ½ ounce/ 17µm base copper	2.4 A	3.4 A
200 mil wide external trace ½ ounce/ 17µm base copper	4.0 A	5.5 A
400 mil wide external trace ½ ounce/ 17µm base copper	7.0 A	10.0 A

3.4.3. VCC5_SBY Routing

The +5V Suspend power rail, if used, should be sized to handle 2A. Most, but not all, Modules will use considerably less than 2A for this power rail. Modules with multiple Ethernet channels and wake-on-LAN capability will use more current. The COM Express Specification allows up to 2A on this rail.

3.4.4. Power State and Reset Signal Routing

Power state and reset signals are single-ended signals that do not have any particular routing constraints.

To utilize the full functionality of PCI Express devices on the COM Express Carrier Board, some additional supply voltages are necessary besides the standard supply voltages of the ATX power supply. Many PCI Express devices are capable of generating wake up events during Suspend operation; for example an external PCI Express Ethernet device that supports 'Wake On LAN' functionality. Therefore, it is necessary to generate an additional 3.3V Suspend voltage on the Carrier Board to supply such devices during Suspend operation. The voltage regulator must be designed to meet the power requirements of the connected devices.

The PCI Express specification defines maximum power requirements for the different PCI Express connectors and/or devices. The power supply for the Carrier Board must be designed to meet these maximum power requirements. Table 44 below shows the maximum current consumption defined for the different types of PCI Express connectors.

Table 44: PCIe Connector Power and Bulk Decoupling Requirements

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
VCC_12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk		
VCC_3V3	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk	1.35A	1.0A
VCC_3V3_SB	375mA @ 150uF bulk	375mA @ 150uF bulk	275mA	330mA
VCC_1V5			750mA	500mA

3.4.5. Slot Card Supply Decoupling Recommendations

Implementing PCI Express connectors on the Carrier Board requires decoupling of the connector supply voltages to reduce possible voltage drops and to provide an AC return path in a manner consistent with high-speed signaling techniques. Decoupling capacitors should be placed as close as possible to the power pins of the connectors. Table 45 below shows the minimum requirements for power decoupling of the different power pin types of each PCI Express connector type.

Table 45: PCIe High Frequency Decoupling Requirements

Power Pin Type	PCIe x1, x4 Connector	PCIe x16 Connector	ExpressCard Connector	PCIe Mini Card Connector
VCC_12V	1x 22µF, 2x 100nF	4x 22uF, 2x 100nF	-	-
VCC_3V3	1x 22uF, 2x 100nF	1x 100uF, 2x 100nF	-	-
VCC_3V3_SB	1x 22uF, 2x 100nF	1x 22uF, 2x 100nF	-	-
VCC_1V5	-	-	-	-

4. BIOS Considerations

4.1. Legacy versus Legacy-Free

For the purposes of this document, “legacy” refers to a set of peripherals provided in desktop PCs and associated chipsets that are no longer in production, including PS/2 keyboard and mouse, parallel port (LPT), and UART serial ports. The COM Express standard was created with newer chipsets in mind. As a result, COM Express is “legacy-free”, which means that legacy peripherals are not directly supported by the module. Such peripherals have been replaced by space-efficient high-speed interfaces such as USB 2.0.

To facilitate the market’s transition toward newer peripherals, the Low Pin Count (LPC) interface was created as a space-efficient replacement for the Industry Standard Architecture (ISA) bus. In addition to firmware devices such as BIOS flash, low-speed super I/O controllers were developed for the LPC bus to fill the gap until the momentum could build for new high-speed-serial-based peripherals.

4.2. Super I/O

Within the COM Express modular architecture, super I/O controllers could be placed on Carrier Boards according to unique application requirements. However, LPC super I/O devices are closely coupled to the BIOS firmware that initializes them and performs setup-based interrupt assignments. The BIOS flash generally resides on the COM Express Modules in order for the Modules to be self-booting. This tight coupling of LPC super I/O to the BIOS presents a multitude of problems in a legacy-free modular environment.

Normally the BIOS vendor supplies to the BIOS developer the choice of different super I/O Modules that can be plugged-in at the source level during the BIOS build process. The BIOS super I/O code Modules often require considerable adaptation work by the BIOS developer to be able to be “plugged-in”. The supported super I/O device would be determined by the Module vendor, and other device support would involve a custom BIOS for each super I/O device.

Consequently, PICMG recommends using USB peripherals or PCI or PCI Express super I/O devices on Carrier Boards for customers wishing to use UART serial ports (COM1, COM2, etc.) or other legacy peripherals. Plug-and-play based interrupt assignments are automatic, and drivers initialize devices after the operating system is loaded. A USB keyboard can be used to enter BIOS setup prior to power-on self-test.

PICMG recommends against using LPC super I/O devices on the Carrier Board, as such usage creates BIOS customization requirements and can greatly restrict Module interoperability. PCI, PCI Express, and/or USB devices should be used instead.

PICMG suggests that alternate BIOS firmware support on the Carrier Board as well as port 0x80 implementations are appropriate uses of the LPC interface on the Carrier Board.

5. COM Express Module Connectors

5.1. Connector Descriptions

A pair of 220-pin COM Express Carrier-Board connectors is available from the vendor in a bridged configuration in which the two 220-pin connectors are held together during assembly by a disposable bridge. The bridge keeps the two connectors aligned, relative to each other, during assembly.

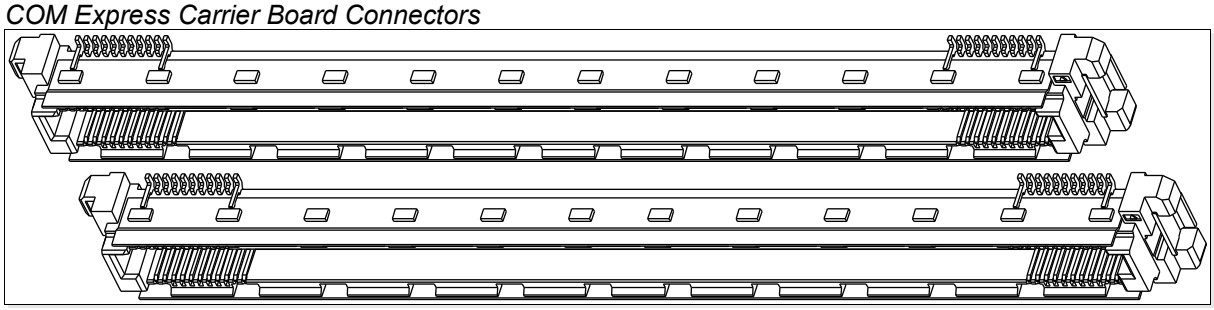
Table 46: COM Express Module Connectors

Type	Height	Partnumber	Note
single connector	5 mm	Tyco 3-1827253-6	FH Series, 220 pos., 0.5mm, Plug
connector pair	5 mm	Tyco 3-1827233-6	FH Series, 440 pos., 0.5mm, Plug, with bridge
single connector	8 mm	Tyco 3-6318491-6	FH Series, 220 pos., 0.5mm, Plug
connector pair	8 mm	Tyco 3-5353652-6	FH Series, 440 pos., 0.5mm, Plug, with bridge

Please check with your Carrier Board manufacturer to determine if single connectors or connector pairs are preferred.

Link: http://catalog.tycoelectronics.com/TE/bin/TE.Connect?C=1&M=BYPN&PID=425179&PN=3-1827233-6&I=13

Figure 53: COM Express Carrier Board Connectors



5.2. Connector Land Patterns and Alignment

It is extremely important that the designers of Carrier Boards ensure that the COM Express connectors have the proper land patterns and that the connectors are aligned correctly. The land pattern is diagrammed in the COM Express Specification. Connector alignment is ensured if the peg location holes in the PCB connector pattern are in the correct positions (as shown in the land pattern of the COM Express Specification) and if the holes are drilled to the proper size and tolerance by the PCB fabricator.

5.3. Connector and Module CAD Symbol Recommendations

The 440-pin COM Express connector should be shown in the Carrier Board CAD system as a single schematic symbol and a single PCB symbol, rather than as a pair of 220-pin symbols. This ensures that the relative position of the two 220-pin connectors remains correct as PCB placement for the Carrier Board is done.

It also is very advantageous to extend this concept to include the COM Express Module outline and the Module mounting holes in the same PCB land pattern. This allows PCB designers to easily move the entire Module around to try placement options without losing the relative positions and orientations of the Module connectors, mounting holes, and Module outline.

6. Carrier Board PCB Layout Guidelines

6.1. General

6.2. PCB Stack-ups

Note ***Section 6 'Carrier Board PCB Layout Guidelines' assumes a thickness for the carrier PCB to be 0.62 inches. Other PCB mechanics are possible but the described Stack-ups need to be adapted.***

6.2.1. Four-Layer Stack-up

Figure 54: Four-Layer Stack-up

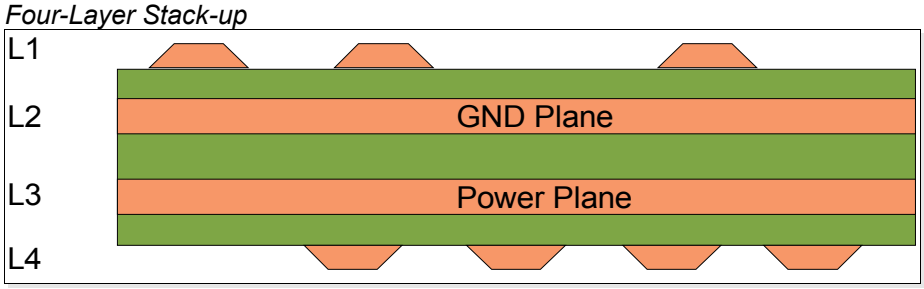


Figure 54 above is an example of a four layer stack-up. Layers L1 and L4 are used for signal routing.

Layers L2 and L3 are used for solid ground and power planes respectively.

Microstrips on Layers 1 and 4 reference ground and power planes on Layers 2 and 3 respectively.

In some cases, it may be advantageous to swap the GND and PWR planes. This allows Layer 4 to be GND referenced. Layer 4 is clear of parts and may be the preferred primary routing layer.

6.2.2. Six-Layer Stack-up

Figure 55: Six-Layer Stack-up

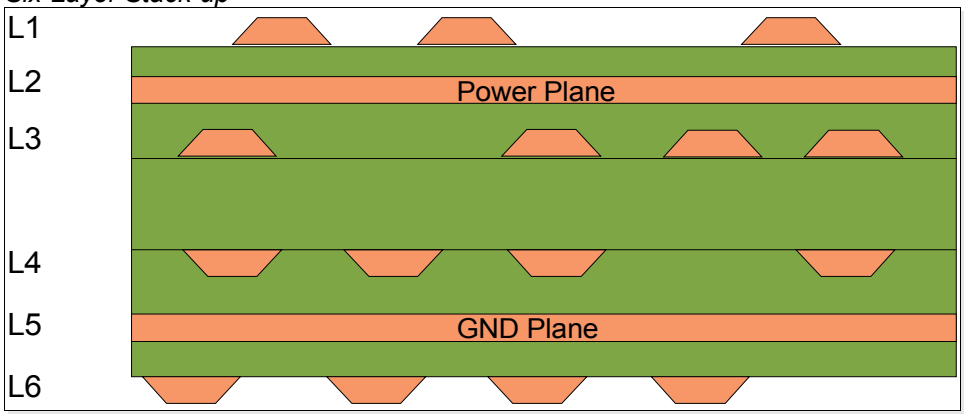


Figure 55 above is an example of a six layer stack-up. Layers L1, L3, L4 and L6 are used for signal-routing. Layers L2 and L5 are power and ground planes respectively.

Microstrips on Layers 1 and 6 reference solid ground and power planes on Layers 2 and 5 respectively.

Inner Layers 3 and 4 are asymmetric striplines that are referenced to planes on Layers 2 and 5.

6.2.3. Eight-Layer Stack-up

Figure 56: Eight-Layer Stack-up

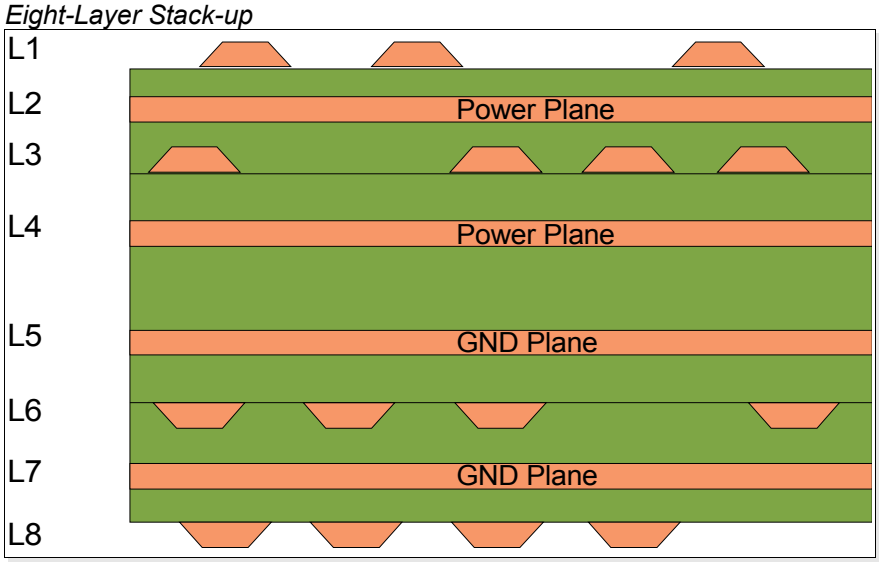


Figure 56 above is an example of an eight layer stack-up. Layers L1, L3, L6 and L8 are used for signal-routing. Layers L2 and L7 are solid ground planes, while L4 and L5 are used for power.

Microstrip Layers 1 and 8 reference solid ground planes on Layers 2 and 7 respectively.

Inner signal Layers 3 and 6 are asymmetric striplines that route differential signals. These signals are referenced to Layers 2 and 7 to meet the characteristic impedance target for these traces.

To reduce coupling to Layers 4 and 5, specify thicker prepreg to increase layer separation.

6.3. Trace-Impedance Considerations

Most high-speed interfaces used in an COM Express design for a Carrier Board are differential pairs that need a well-defined and consistent differential and single-ended impedance. The differential pairs should be edge-coupled (i.e. the two lines in the pair are on the same PCB layer, at a consistent spacing to each other). Broadside coupling (in which the two lines in the pair track each other on different layers) is not recommended for mainstream commercial PCB fabrication.

There are two basic structures used for high-speed differential and single-ended signals. The first is known as a “microstrip”, in which a trace or trace pair is referenced to a single ground or power plane.

The outer layers of multi-layer PCBs are microstrips. A diagram of a microstrip cross section is shown in Figure 57 'Microstrip Cross Section' below.

The second structure is the “stripline”, in which a trace or pair of traces is sandwiched between two reference planes, as shown in Figure 58 'Strip Line Cross Sectionbelow' below. If the traces are exactly halfway between the reference planes, then the stripline is said to be symmetric or balanced. Usually the traces are a lot closer to one of the planes than the other (often because there is another orthogonal trace layer, which is not shown in Figure 58 'Strip Line Cross Section' below). In this case, the striplines are said to be asymmetric or unbalanced. Inner layer traces on multi-layer PCBs are usually asymmetric striplines.

Before proceeding with a Carrier Board layout, designers should decide on a PCB stack-up and on trace parameters, primarily the trace-width and differential-pair spacing. It is quite a bit harder to change the differential impedance of a trace pair after layout work is done than it is to change the impedance of a single-ended signal. That is because (with reference to Figure 57 'Microstrip Cross Section' below, Figure 58 'Strip Line Cross Section' below, Table 47 'Trace Parameters' below) the geometric factors that have the biggest impact on the impedance of a single-ended trace are H1 and W1.

Both H1 and W1 can be manipulated slightly by the PCB vendor. The differential impedance of a trace pair depends primarily on H1, W1 and the pair pitch. A PCB vendor can easily manipulate H1 and W1 but changing the pair pitch cannot generally be done at fabrication time. It is more important for the PCB designer and the Project Engineer to determine the routing parameters for differential pairs ahead of time.

Work with a PCB vendor on a suitable board stack-up and do your own homework using a PCB-impedance calculator. An easy to use and comprehensive calculator is available from Polar Instruments (www.polarinstruments.com). Many PCB vendors use software from Polar Instruments for their calculations. Polar Instruments offers an impedance calculator on a low-cost, per-use basis. To find this, search the Web for a “Polar Instruments subscription”. Alternatively, impedance calculators are included in many PCB layout packages, although these are often incomplete when it comes to differential-pair impedances. There also are quite a few free impedance calculators available on the Web. Most are very basic, but they can be useful.

Figure 57: Microstrip Cross Section

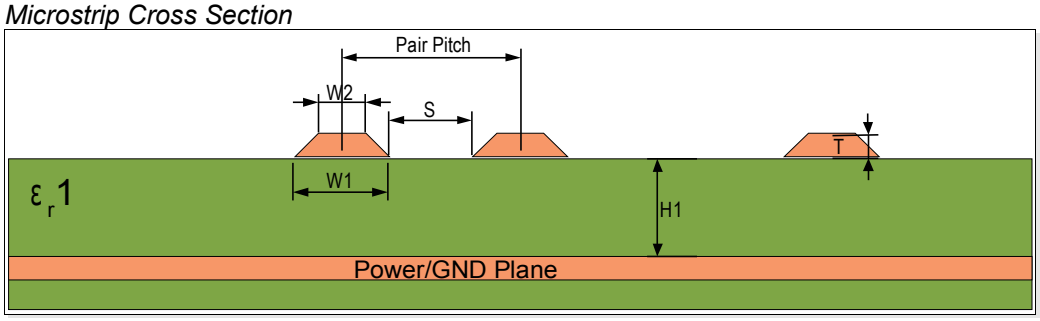


Figure 58: Strip Line Cross Section

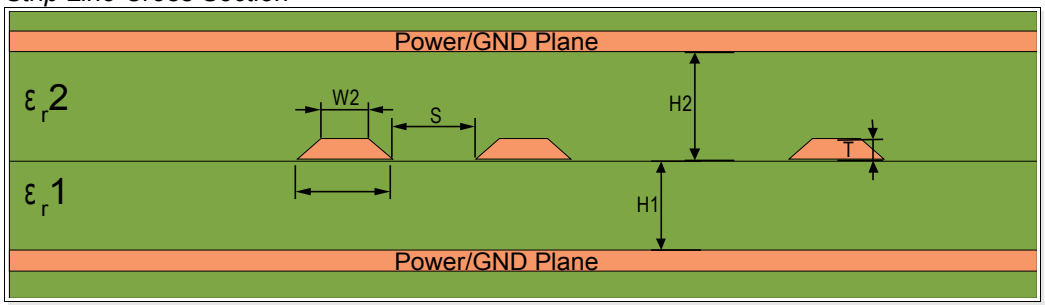


Table 47: Trace Parameters

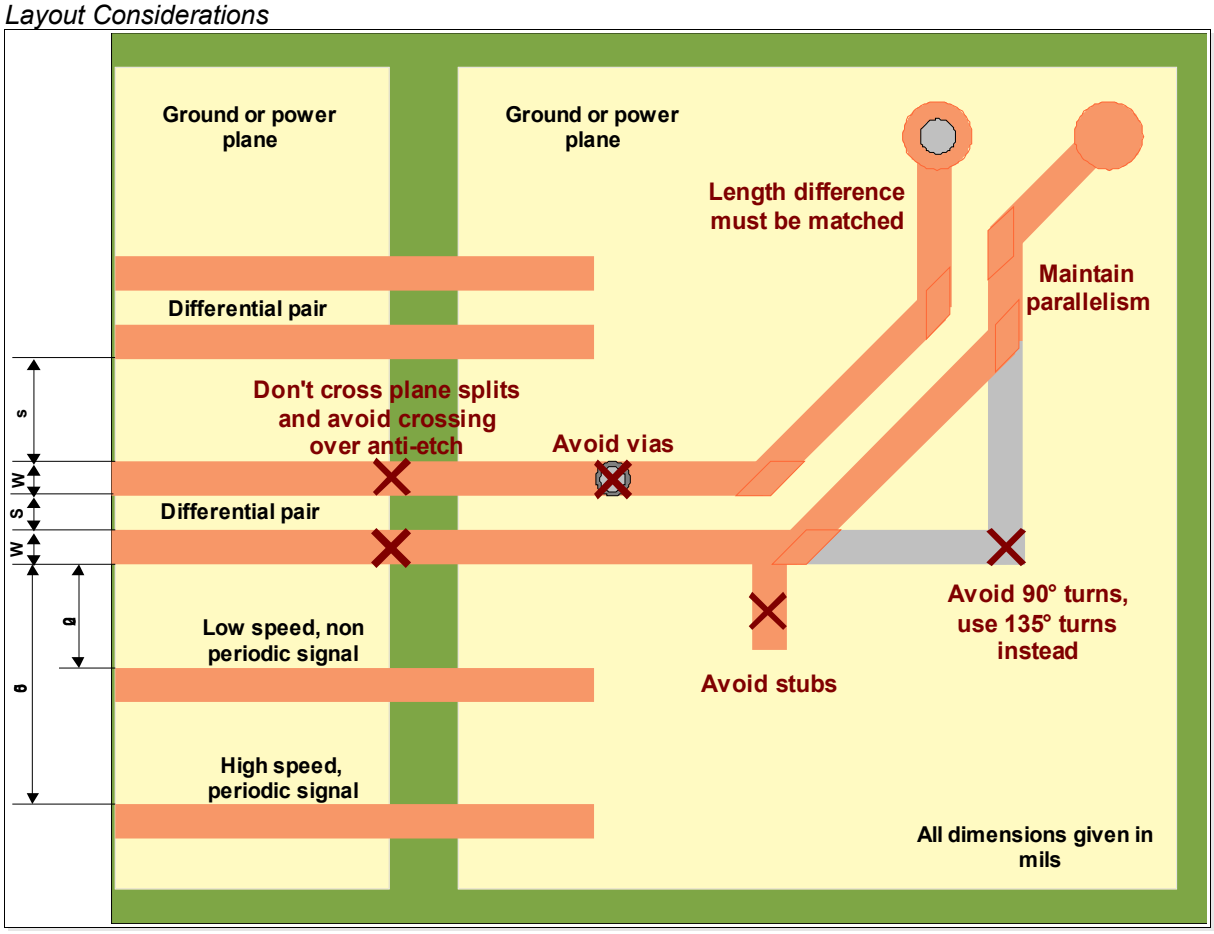
Symbol	Definition
ε_r1	Dielectric constant of material between the trace and the reference plane. Increasing ε_r1 results in a lower trace impedance.
ε_r2	Dielectric constant of the material between the 2nd reference plane (stripline case only). Usually ε_r1 and ε_r2 are the same. Increasing ε_r2 results in a lower trace impedance.
H1	Distance between the trace lower surface and the closer reference plane. Increasing H1 raises the trace impedance (assuming that H1 is less than H2).
H2	Distance between the trace lower surface and the more distant reference plane (stripline case only). Usually H2 is significantly greater than H1. When this is true, the lower plane shown in the figure is the primary reference plane. Increasing H2 raises the trace impedance.
Pair Pitch	The center-to-center spacing between two traces in a differential pair. Increasing the pair pitch raises the differential trace impedance.
S	The spacing or gap between two traces in a differential pair. The pair pitch is the sum of S and W1. Increasing S raises the differential trace impedance.
T	The thickness of the trace. The thickness of a ½ oz. inner layer trace is about 0.0007 inches. The thickness of a 1 oz. inner layer trace is about 0.0014 inches. Outer layer traces using a given copper weight are thicker, due to plating that is usually done on outer layers. Increasing the trace thickness lowers trace impedance.
W1, W2	W1 is the base thickness of the trace. W2 is the thickness at the top of the trace. The relation between W1 and W2 is called the “etch factor” in the PCB trade. For rough calculations, it can be assumed that W1 = W2. The etch factor is process dependent. W2 is often about 0.001 inches less than W1 for ½ oz inner layer traces; for example, a 5 mil (0.005 inch) nominal trace will be 5-mil wide at the bottom and 4-mil wide at the top. Increasing the trace-width lowers trace impedance.

6.4. Routing Rules for High-Speed Differential Interfaces

The following is a list of suggestions for designing with high-speed differential signals. This should help implement these interfaces while providing maximum COM Express Carrier Board performance.

- Use controlled impedance PCB traces that match the specified differential impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing needed to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs and any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- It is best to put CMOS/TTL and differential signals on a different layer(s), which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate, clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.
- Use a minimum of 20mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.

Figure 59: Layout Considerations



In order to determine the necessary trace width, trace height and spacing needed to fulfill the requirements of the interface specification, it's necessary to use an impedance calculator.

6.4.1. PCI Express 1.1 Trace Routing Guidelines

Table 48: PCI Express 1.1 Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate / PCIe Lane	2.5 GBit/s
Maximum signal line length (coupled traces)	TX and RX path: 21.0 inches
Signal length allowance on the COM Express Carrier Board	TX and RX path: 15.85 inches @ 0.28dB/GHz/inch to PCIe device 9.00 inches @ 0.28dB/GHz/inch to PCIe slot
Differential Impedance	92 Ω +/-10% (covers Gen1 100 Ω +/-20% and Gen2 85 Ω +/-20% requirements)
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	4 mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency.
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5mils
Length matching between reference clock pairs (inter-pair)	No electrical requirements.
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.4.2. USB Trace Routing Guidelines

Table 49: USB Trace Routing Guidelines

Parameter	Trace Routing
Transfer rate / Port	480 MBit/s
Maximum signal line length (coupled traces)	Max. 17.0 inches
Signal length used on COM Express Module (including the COM Express connector)	3.0 inches
Signal length allowance for the COM Express Carrier Board	14.0 inches
Differential Impedance	90 Ω +/-15%
Single-ended Impedance	45 Ω +/-10%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	6mils (microstrip routing) (*)
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils
Reference plane	GND referenced preferred
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.4.3. PEG 1.1 Trace Routing Guidelines

Please refer to Section 6.4.1. 'PCI Express 1.1 Trace Routing Guidelines' on page 132

Note ***The COM Express specification does not define different trace routing rules for PEG and PCI Express lanes. Newer chipsets feature low power modes for the PEG signals. In order to ensure compatibility it's recommended to keep the PEG signal lines as short as possible. A max of 5” to the carrier device down and 4” to a carrier slot is advisable.***

6.4.4. SDVO Trace Routing Guidelines

Table 50: SDVO Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate / SDVO Lane	Up to 2.0 GBit/s
Maximum signal line length (coupled traces)	7 inches
Signal length used on COM Express Module (including the Carrier Board connector)	2 inches
Signal length allowance for the COM Express Carrier Board	5 inches to SDVO device
Differential Impedance	100 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5 mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7 mils (microstrip routing) (*)
Spacing between pairs-to-pair	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between differential pairs (inter-pair)	Keep difference within a 2.0 inch delta.
Length matching between differential signal pair and differential clock pair	Max. 5mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 4 vias per differential signal trace
AC coupling capacitors	AC coupling capacitors on the signals 'SDVO_INT+' and 'SDVOINT-' have to be implemented on the customer COM Express Carrier Board, if the device is directly located on the carrier board. When using a slot at the carrier board the capacitors are located at the addon card. Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.4.5. LAN Trace Routing Guidelines

Table 51: LAN Trace Routing Guidelines

Parameter	Trace Routing
Signal length allowance for the COM Express Carrier Board	5.0 inches from the COM Express Module to the magnetics Module
Maximum signal length between isolation magnetics Module and RJ45 connector on the Carrier Board	1.0 inch
Differential Impedance	95 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials. Also observe trace geometry definitions and restrictions provided by the PHY device vendor.***

6.4.6. Serial ATA Trace Routing Guidelines

Table 52: Serial ATA Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	3.0 GBit/s
Maximum signal line length (coupled traces)	7.0 inches on PCB (COM Express Module and Carrier Board. The length of the SATA cable is specified between 0 and 40 inches)
Signal length used on COM Express Module (including the COM Express Carrier Board connector)	2 inches
Signal length available for the COM Express Carrier Board	3 inches
Differential Impedance	100 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between differential pairs (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements. Keep difference within a 3.0 inch delta to minimize latency. Do not serpentine to meet trace length guidelines for the RX and TX path.
Spacing from edge of plane	Min. 40mils
Via Usage	Try to minimize number of vias
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are incorporated on the COM Express Module.

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.4.7. LVDS Trace Routing Guidelines

Table 53: LVDS Trace Routing Guidelines

Parameter	Trace Routing
Maximum signal line length to the LVDS connector (coupled traces)	8.75 inches
Signal length used on COM Express Module (including the COM Express Carrier Board connector)	2.0 inches
Signal length to the LVDS connector available for the COM Express Carrier Board	6.75 inches
Differential Impedance	100 Ω +/-20%
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	4mils (microstrip routing) (*)
Spacing between differential pair signals (intra-pair) (S)	7mils (microstrip routing) (*)
Spacing between pair to pairs (inter-pair) (s)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	+/- 20mils
Length matching between clock and data pairs (inter-pair)	+/- 20mils
Length matching between data pairs (inter-pair)	+/- 40mils
Spacing from edge of plane	+/- 40mils
Reference plane	GND referenced preferred
Via Usage	Max. of 2 vias per line

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.5. Routing Rules for Single Ended Interfaces

The following is a list of suggestions for designing with single ended signals. This should help implement these interfaces while providing maximum COM Express Carrier Board performance.

- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use or generate clocks.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Stubs on signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.
- Route all traces over continuous planes with no interruptions (ground reference preferred). Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.
- Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.

6.5.1. PCI Trace Routing Guidelines

Table 54: PCI Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate @ 33MHz	132 MB/sec
Maximum data and control signal length allowance for the COM Express Carrier Board.	10 inches
Maximum clock signal length allowance for the COM Express Carrier Board.	8.88 inches
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between signals (inter-signal) (S)	7mils (microstrip routing) (*)
Length matching between single ended signals	Max. 200mils
Length matching between clock signals	Max. 200mils
Spacing from edge of plane	Min. 40mils
Reference plane	GND referenced preferred
Via Usage	Try to minimize number of vias
Decoupling capacitors for each PCI slot.	Min. 1x22µF, 2x 100nF @ VCC 5V Min. 2x22µF, 4x 100nF @ VCC 3.3V Min. 1x22µF, 2x 100nF @ +12V (if used) Min. 1x22µF, 2x 100nF @ -12V (if used) The decoupling capacitors for the power rails should be placed as close as possible to the slot power pins, connected with wide traces.

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.5.2. IDE Trace Routing Guidelines

Table 55: IDE Trace Routing Guidelines

Parameter	Trace Routing
Maximum Transfer Rate @ ATA100	100 MB/sec
Maximum length allowance for signals on the COM Express Carrier Board @ ATA100.	7.0 inches
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between signals (inter-signal) (S)	7mils (microstrip routing) (*)
Length matching between strobe and data signals	Max. 450mils
Length matching between data signals	Max. 200mils
Length matching between strobe signals 'IDE_IOR' and 'IDE_IOW'.	Max. 100mils
Spacing from edge of plane	Min. 40mils
Reference plane	GND referenced preferred
Via Usage	Try to minimize number of vias

Note ***Suggested trace parameters shown. Use of impedance calculation software is recommended to determine trace width, distance to reference planes, and pair spacing applicable to your specific project and PCB materials.***

6.5.3. LPC Trace Routing Guidelines

Table 56: LPC Trace Routing Guidelines

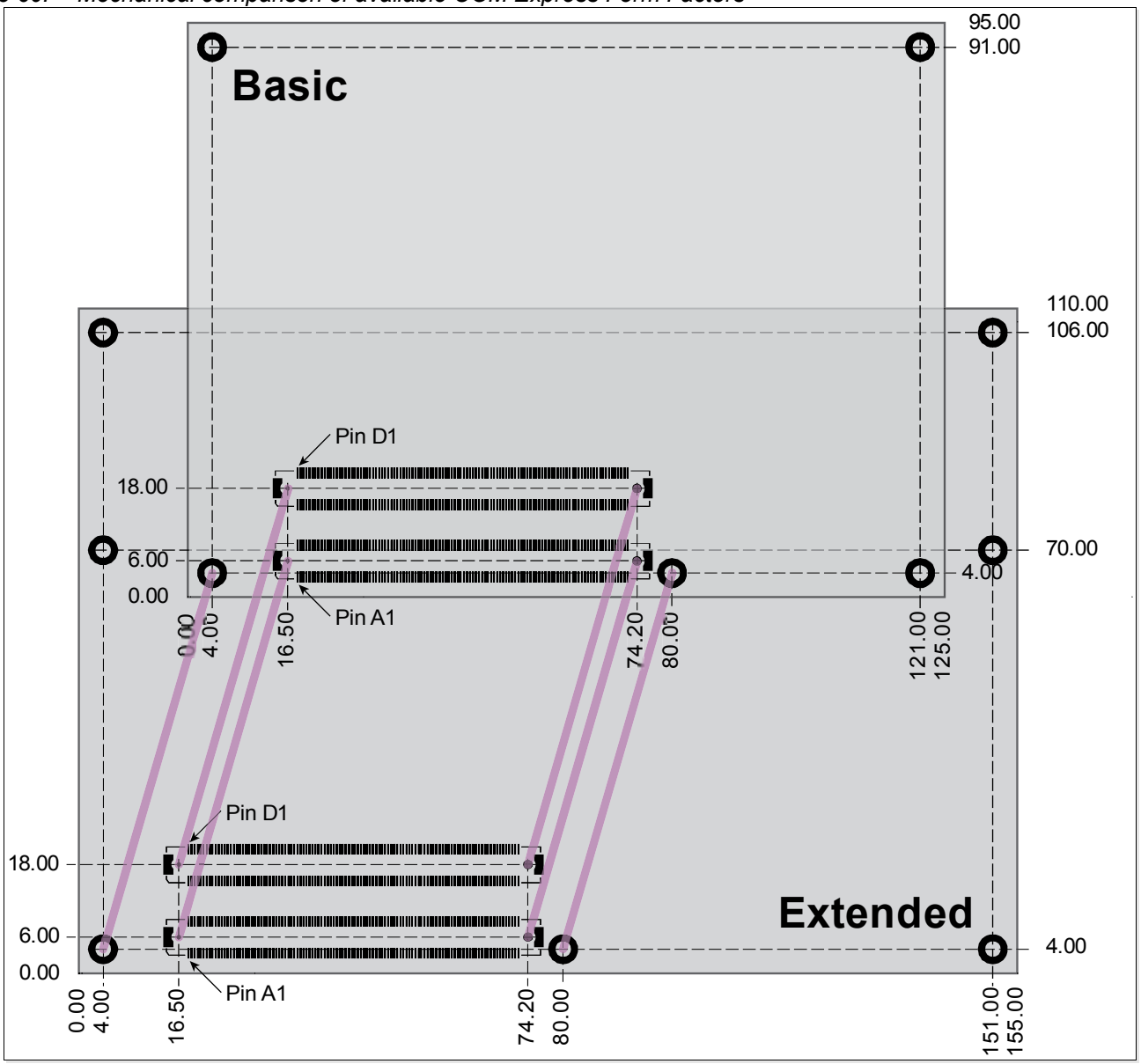
Parameter	Trace Routing
Transfer Rate @ 33MHz	16 MBit/s
Maximum data and control signal length allowance for the COM Express carrier board	15.0 inches
Maximum clock signal length allowance for the COM Express carrier board	8.88 inches
Single-ended Impedance	55 Ω +/-15%
Trace width (W)	5mils (microstrip routing) (*)
Spacing between signals (inter-signal) (S)	7mils (microstrip routing) (*)
Length matching between single ended signals	Max. 200mils
Length matching between clock signals	Max. 200mils
Spacing from edge of plane	Min. 40mils
Reference plane	GND referenced preferred
Via Usage	Try to minimize number of vias

7. Mechanical Considerations

7.1. Form Factors

The COM Express specification describes 2 different sized COM Express Modules. The Basic (95x125mm²) and the Extended (110x155mm²). Based on customer demand, many COM Express Module vendors also offer even smaller form factors with backwards compatibility to the COM Express specification.

Figure 60: Mechanical comparison of available COM Express Form Factors



7.2. Heatspreader

An important factor for each system integration is the thermal design. The heatspreader acts as a thermal coupling device to the Module. Usually It is a 3mm thick aluminum plate.

The heatspreader is thermally coupled to the CPU via a thermal gap filler and on some Modules it may also be thermally coupled to other heat generating components with the use of additional thermal gap fillers.

Although the heatspreader is the thermal interface where most of the heat generated by the Module is dissipated, it is not to be considered as a heatsink. It has been designed to be used as a thermal interface between the Module and the application specific thermal solution. The application specific thermal solution may use heatsinks with fans, and/or heat pipes, which can be attached to the heatspreader. Some thermal solutions may also require that the heatspreader is attached directly to the systems chassis therefore using the whole chassis as a heat dissipater.

The main mechanical mounting solutions for systems based on COM Express Modules have proven to be the 'top-mounting' and 'bottom-mounting' solutions. The decision as to which solution will be used is determined by the mechanical construction and the cooling solution of the customer's system. There are two variants of the heatspreader, one for each mounting possibility. One version has threaded standoffs and the other has non-threaded standoffs (bore hole). The following sections describe these two common mounting possibilities and the additional components (standoffs, screws, etc...) that are necessary to implement the respective solution.

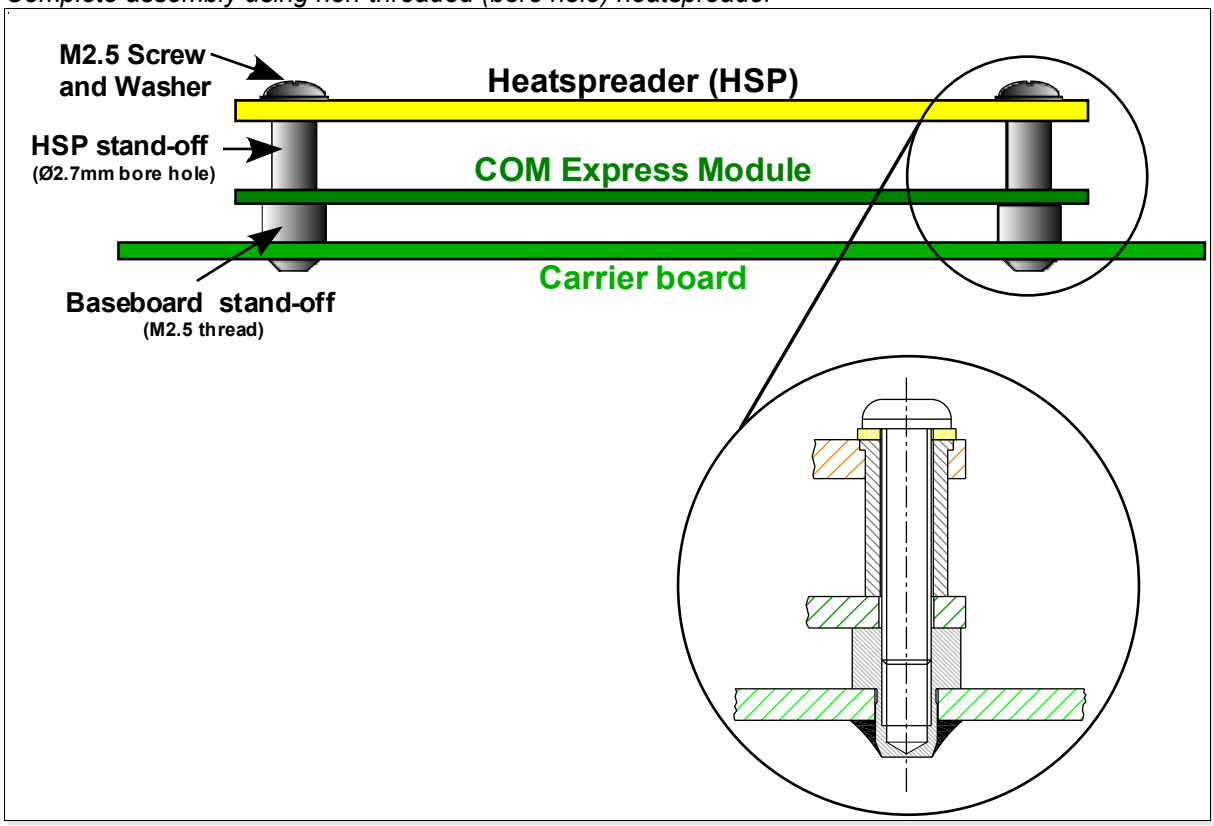
The examples shown in the following Sections 7.2.1 'Top mounting' and 7.2.2. 'Bottom mounting' are for heatspreader thermal solutions only. Other types of thermal solutions are possible that might require other mounting methods.

7.2.1. Top mounting

For top mounting heatspreaders with non-threaded standoffs (bore hole) are used.

This variant of the heatspreader was designed to be used in a system where the heatspreader screws need to be inserted from the top side of the complete assembly. In this case the threads for securing the screws are in the Carrier Board's standoffs. This is the reason why the heatspreader must have non-threaded (bore hole) standoffs.

Figure 61: Complete assembly using non-threaded (bore hole) heatspreader



Note ***The torque specification for heatspreader screws is 0.5 Nm.***

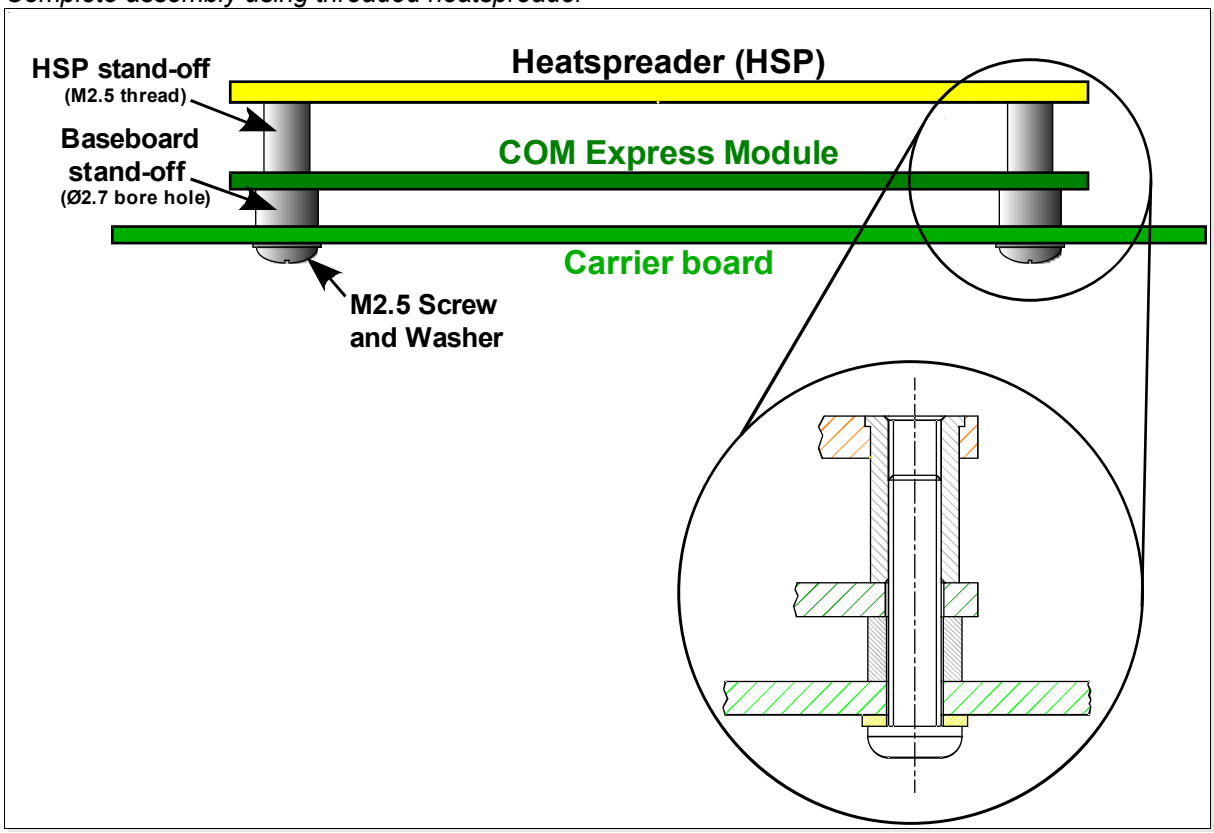
Caution ***Do not use a threaded heatspreader together with threaded Carrier Board standoffs. The combination of the two threads may be staggered, which could lead to stripping or cross-threading of the threads in either the standoffs of the heatspreader or Carrier Board.***

7.2.2. Bottom mounting

Heatspreaders with threaded standoffs are used for bottom-mounting solutions.

This variant of the heatspreader has been designed to be used in systems where the heatspreader screws need to be inserted from the bottom side of the complete assembly. For this solution a heatspreader version with threaded standoffs must be used. In this case, the standoffs used on the Carrier Board are not threaded.

Figure 62: Complete assembly using threaded heatspreader



Note ***The torque specification for heatspreader screws is 0.5 Nm.***

Caution ***Do not use a threaded heatspreader together with threaded Carrier Board standoffs. The combination of the two threads may be staggered, which could lead to stripping of the threads in either the standoffs of the heatspreader or Carrier Board.***

7.2.3. Materials

Independently from the above mentioned mounting methods the material from the tables below is required to mount a COM Express Module to a Carrier Board.

Table 57: Heatspreader mounting material needed (5mm connectors at the Carrier Board)

Component	Quantity	Comment
M2,5 x 16mm screw[1]	5	Recessed raised cheese head screw with point, galvanized with metric thread M2,5 and 16mm length DIN7985 / ISO7045
Washer .2,7mm	5	Plain washer galvanized for M2,5 DIN433 / ISO7092

Table 58: Heatspreader mounting material needed (8mm connectors at the Carrier Board)

Component	Quantity	Comment
M2,5 x 19mm screw	5	Recessed raised cheese head screw with point, galvanized with metric thread M2,5 and 19mm length DIN7985 / ISO7045
Washer .2,7mm	5	Plain washer galvanized for M2,5 DIN433 / ISO7092

Table 59: Carrier board standoffs

Component	Mounting Type	Comment
5mm, press in, M2.5	Top	EFCO ECM00593-L, www.efcotec.com/product.asp?pid=102
5mm, press in, Ø2.7mm	Bottom	EFCO ECM00592-L, www.efcotec.com/product.asp?pid=102
5mm, solder, M2.5	Top	EFCO ECM00530-L, www.efcotec.com/product.asp?pid=102
8mm, press in, M2.5	Top	EFCO ECM00594L, www.efcotec.com/product.asp?pid=102
8mm, press in, Ø2.7mm	Bottom	EFCO ECM00588-L, www.efcotec.com/product.asp?pid=102
5mm, solder, M2.5	Top	EFCO ECM00579-L, www.efcotec.com/product.asp?pid=102
5mm spacer	Bottom	div.
8mm spacer	Bottom	div.
5mm spacer + nut	Top	div.
8mm spacer + nut	Top	div.

1 The ideal length of the mounting screws is 17mm. As this length is not easy available the 16mm version can be used as a replacement.

8. Applicable Documents and Standards

8.1. Technology Specifications

Table 60: Reference specifications

Specification	Description	Link
1000BASE T	IEEE standard 802.3ab 1000BASE T Ethernet	www.ieee.org/portal/site
AC'97	Audio Codec '97 Component Specification, Version 2.3	download.intel.com/support/motherboards/desktop/sb/ac97_r23.pdf
ACPI	Advanced Configuration and Power Interface Specification Rev. 3.0a	www.acpi.info
ATA	ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002.	www.ansi.org www.t13.org
ATX power	ATX power supply design guide	www.intel.com
CF-Card	CF+ and CompactFlash Specification, Revision 4.1, February 16, 2007, Copyright © Compact Flash Association.	www.compactflash.org
COM Express	PICMG® COM Express Module™ Base Specification	www.picmg.org
COM.0	PICMG COM.0 R1.0, "COM Express Module Base Specification", July 10, 2005	www.picmg.org
DDC	Enhanced Display Data Channel Specification Version 1.1 (DDC)	www.vesa.org
DisplayID	DisplayID Ver 1.0	www.vesa.org
DVI	Digital Visual Interface, Rev 1.0, April 2, 1999, Digital Display Working Group	www.ddwg.org
EDID	Extended Display Identification Data Standard Version 1.3 (EDID™)	www.vesa.org
ExpressCard	ExpressCard Standard Release 1.0	www.expresscard.org
HDA	High Definition Audio Specification, Rev. 1.0	www.intel.com/standards/hdaudio
I2C	The I2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1	www.nxp.com
IEEE 802.3-2002	IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications	www.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1 (LPC)	www.intel.com/design/chipsets/industry/lpc.htm
LVDS	Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor	www.national.com
LVDS	LVDS Owner's Manual	www.national.com
LVDS	ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001.	www.ansi.org
mini-PCI Express Card	PCI Express Mini Card Electromechanical Specification 1.2	www.pcisig.com/specifications/pciexpress/base
PATA	Parallel ATA [IDE]	www.t13.org
PCI	PCI Local Bus Specification, Revision 2.3	www.pcisig.com/specifications
PCI Express	PCI Express Base Specification, Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved	www.pcisig.com
PCI Express	PCI Express Base Specification, Revision 2.0	www.pcisig.com/specifications

Specification	Description	Link
PCI Express	Mobile Graphics Low-Power Addendum to the PCI Express Base Specification, Rev. 1.0	www.pcisig.com
PCI Express Card	PCI Express Card Electromechanical Specification, Rev. 1.1 Section 2.	www.pcisig.com/specifications
PCI Express Mini Card	PCI Express Mini Card Electromechanical Specification, PCI Special Interest Group	www.pcisig.com
SATA	Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved	www.sata-io.org
SATA	Serial ATA Specification, Revision 1.0a	www.serialata.org
SDVO	Intel NDA is required	
SMBUS	System Management Bus (SMBUS) Specification, Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved	www.smbus.org
Smart Battery	Smart Battery Data Specification, Revision 1.1, December 11, 1998	www.sbs-forum.org
USB	Universal Serial Bus Specification, Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc, Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved	www.usb.org
USB	PoweredUSB Electro/Mechanical 050121 (0.8g), 2005	www.poweredusb.org

8.2. Regulatory Specifications

FCC Rules Part 15 Class B devices

EN 61000-4-2 Personnel Electrostatic Discharge Immunity Testing

8.3. Useful books

Table 61: Useful books

Title	Author	Note
PCI Express System Architecture	Ravi Budruk, Don Anderson, Tom Shanley	www.mindshare.com
PCI System Architecture (4th Edition)	Tom Shanley, Don Anderson	www.mindshare.com
Universal Serial Bus System Architecture	Don Anderson	www.mindshare.com
SATA Storage Technology	Don Anderson	www.mindshare.com
Protected Mode Software Architecture (The PC System Architecture Series)	Tom Shanley	www.mindshare.com
The Unabridged Pentium 4	Tom Shanley	www.mindshare.com
Building the Power-Efficient PC: A Developer's Guide to ACPI Power Management, First Edition	Jerzy Kolinski, Ram Chary, Andrew Henroid, and Barry Press	Intel Press, 2002, ISBN 0-9702846-8-3
Hardware Bible	Winn L. Rosch	SAMS, 1997, 0-672-30954-8
The Indispensable PC Hardware Book	Hans-Peter Messmer	Addison-Wesley, 1994, ISBN 0-201-62424-9
The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition	John P. Choisser and John O. Foster	Annabooks, 1997, ISBN 0-929392-36-1
PC Hardware in a Nutshell, 3rd Edition	Robert Bruce Thompson and Barbara Fritchman Thompson	O'Reilly, 2003, ISBN 0-596-00513-X
PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition	Edward Solari and George Willse	Annabooks, Intel Press, 2001, ISBN 0-929392-63-9
PCI System Architecture	Tom Shanley and Don Anderson	Addison-Wesley, 2000, ISBN 0-201-30974-2
PCI Express Electrical Interconnect Design: Practical Solutions for Board-level Integration and Validation, First Edition	Dave Coleman, Scott Gardiner, Mohamad Kolberhdari, and Stephen Peters	Intel Press, 2005, ISBN 0-9743649-9-1
Introduction to PCI Express: A Hardware and Software Developer's Guide, First Edition	Adam Wilen, Justin Schade, and Ron Thornburg	Intel Press, 2003, ISBN 0-9702846-9-1
Serial ATA Storage Architecture and Applications, First Edition	Knut Grimsrud and Hubbert Smith	Intel Press, 2003, ISBN 0-9717861-8-6
USB Design by Example, A Practical Guide to Building I/O Devices, Second Edition	John Hyde	Intel Press, ISBN 0-9702846-5-9
Universal Serial Bus System Architecture, Second Edition	Don Anderson and Dave Dzatko	Mindshare, Inc., ISBN 0-201-30975-0
Printed Circuits Handbook, Fourth Edition	Clyde F. Coombs Jr.	McGraw-Hill, 1996, ISBN 0—07-012754-9
High Speed Signal Propagation, First Edition	Howard Johnson and Martin Graham	Prentice Hall, 2003, ISBN 0-13-084408-X
High Speed Digital Design: A Handbook of Black Magic, First Edition	Howard Johnson	Prentice Hall, ISBN: 0133957241
C Programmer's Guide to Serial Communications, Second Edition	Joe Campbell	SAMS, 1987, ISBN 0-672-22584-0
The Programmer's PC Sourcebook, Second Edition	Thom Hogan	Microsoft Press, 1991, ISBN 1-55615-321-X
The Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas	Frank van Gilluwe	Addison-Wesley, 1997, ISBN 0-201-47950-8
VHDL Modeling for Digital Design Synthesis	Yu-Chin Hsu, Kevin F. Tsai, Jessie T. Liu and Eric S. Lin	Kluwer Academic Publishers, 1995, ISBN: 0-7923-9597-2

Appendix A: Sourcecode for Port 80 Decoder

```
-- IO80 catcher for LPC bus.
-- File:  LPC_IOW80_1.1.VHD
-- Revision:  1.1
-- Author:   Eric Leonard (partially based on Nicolas Gonthier's T3001)
--          Subsequent modifications by:
--                Detlef Herbst and Travis Evans - 08/10/05
-- Decode only I/O writes to 80h
-- Features:
--    - I/O 80 access only (internally decoded)
--    - No support for read, only write.
--    - All signals synchronous to LPC clock
-- Notes:
--    - Unless otherwise noted, all signals are active high.
--    - Suffix "n" indicate active low logic.
--
--    - Successfully implemented on Brownsville baseboard with Seven Segment
--    - display P/N SA39-11 (common Anode - Low turns on segment) from Kingbright
-- Related documents:
--           - Low Pin Count (LPC) Interface Specification, Revision 1.0 (sept 1997)
--------------------------------------------------------------------------------
library IEEE;
use IEEE.std_logic_1164.all;

entity LPC_IOW80 is port (
  lclk:          in     std_logic;                    -- LPC: 33MHz clock (rising edge)
  lframe_n:      in     std_logic;                    -- LPC: frame, active low
  lreset_n:in    std_logic;                    -- LPC: reset, active low
  lad:           in     std_logic_vector(3 downto 0);-- LPC: multiplexed bus
  seven_seg_L:   out    std_logic_vector(7 downto 0);-- SSeg Data output
  seven_seg_H:   out    std_logic_vector(7 downto 0)  -- SSeg Data output
);
end LPC_IOW80;

architecture RTL of LPC_IOW80 is

        type LPC_State_Type is (
                IDLE,           -- Waiting for a start condition
                START,          -- Start condition detected
                WADDN3,                 -- I/O write address nibble 3 (A15..A12)
                WADDN2,                 -- I/O write address nibble 2 (A11..A8 )
                WADDN1,                 -- I/O write address nibble 1 (A7..A4)
                WADDN0,                 -- I/O write address nibble 0 (A3-A0)
                WDATN1,                 -- I/O write data nibble 0 (D7..D4)
                WDATN0,                 -- I/O write data nibble 1 (D3..D0)
                WHTAR0,                 -- I/O write host turn around phase 0
                WHTAR1,                 -- I/O write host turn around phase 1
                WSYNC,          -- I/O write sync
                WPTAR );        -- I/O write peripheral turn around

        signal LPC_State: LPC_State_Type;

        signal lframe_nreg: std_logic;                          -- LPC frame register
        signal lad_rin:         std_logic_vector(lad'range);   -- LPC input registers
        signal W_Data:          std_logic_vector(7 downto 0);           -- LPC input Post Code

begin

--------------------------------------------------------------------------------
-- LPC bidirectional pins definition.
--------------------------------------------------------------------------------

-- Input register to get some timing margin
P_input_register: process(lclk)
begin
        if (lclk'event and lclk='1') then
                lad_rin     <= lad;
                lframe_nreg <= lframe_n;
        end if;
end process;
```

```
--------------------------------------------------------------------------------
-- LPC state machine
-- LPC_State value is actually one clock cycle late.
--------------------------------------------------------------------------------
P_LPC_StatMachine: process(lclk)

begin
  if (lclk'event and lclk='1') then

-- Synchronous reset
          if (lreset_n = '0') then
                    LPC_State <= IDLE;
                    W_Data(7 downto 0) <= "00000000";    -- init. both displays to all on
                    else
                              case LPC_State is

                               -- Looking for a START condition
                               when IDLE =>

                                        if (lframe_nreg = '0') and (lad_rin = "0000") then
                                                  LPC_State <= START;          -- START condition detected
                                                  end if;

                                        -- Skip extra cycles on START frame
-- (can be many clock cycles)
                                        -- and then, check for I/O write transaction
                                 when START =>
                                                  if (lframe_nreg = '0') then -- frame still asserted
                                                            if (lad_rin /= "0000") then
                                                            LPC_State <= IDLE; -- unsupported start code
                                                            end if;
                                                  else
                                                  if (lad_rin(3 downto 1) = "001") then
                                                            LPC_State <= WADDN3;       -- I/O write detected
                                                            else
                                                            LPC_State <= IDLE;            -- unsupported command
                                                            end if;
                                                  end if;

                                        -- ---------------------------------
                                        -- I/O write transaction processing
                                        -- ---------------------------------
                                        when WADDN3 => -- Write Data Address Nibble 3

                                                  -- Find next state
                                                  if (lframe_nreg = '0') or (lad_rin /= "0000") then
LPC_State <= IDLE; -          -- abort cycle, bad frame
-- or address mismatch
                                                  else
                                                            LPC_State <= WADDN2;
                                                  end if;

                                        when WADDN2 =>              -- Write Data Address Nibble 2

                                                  -- Find next state
                                                  if (lframe_nreg = '0') or (lad_rin /= "0000") then
LPC_State <= IDLE; -- abort cycle, bad frame
   -- or address mismatch
                                                  else
                                                            LPC_State <= WADDN1;
                                                  end if;

                                        when WADDN1 =>              -- Write Data Address Nibble 1

                                                  -- Find next state
                                                  if (lframe_nreg = '0') or (lad_rin /= "1000") then
LPC_State <= IDLE; -- abort cycle, bad frame
   -- or address mismatch
                                                  else
                                                            LPC_State <= WADDN0;
                                                  end if;

                                        when WADDN0 =>              -- Write Data Address Nibble 0

                                                  -- Find next state
                                                  if (lframe_nreg = '0') or (lad_rin /= "0000") then
```

```
LPC_State <= IDLE; -- abort cycle, bad frame
    -- or address mismatch
                                        else
                                        -- Write address valid. Subsequent Data displays.
LPC_State <= WDATN0;        -- Next state will get
-- first data nibble
                                        end if;

when WDATN0 =>  -- Data LSN (Least Significant Nibble)is
-- sent first
                                        W_Data(3 downto 0) <= lad_rin; -- latch data (LSN)
                                        if (lframe_nreg = '1') then
 LPC_State <= WDATN1; ¬¬¬-- Next state gets
 -- 2nd data nibble
                                        else
                                                LPC_State <= IDLE;
                                        end if;

                                    when WDATN1 =>   -- Data MSN (Most Significant Nibble)
                                        W_Data(7 downto 4) <= lad_rin; -- latch data (MSN)
                                        if (lframe_nreg = '1') then
                                                LPC_State <= WHTAR0;
                                        else
                                                LPC_State <= IDLE;
                                        end if;

                                    when WHTAR0 =>   -- Write Data Turn Around Cycle 0

                                        if (lframe_nreg = '1') and (lad_rin = "1111") then
                                                LPC_State <= WHTAR1;
                                        else
                                                LPC_State <= IDLE;
                                        end if;

                                    when WHTAR1 =>    -- Write Data Turn Around Cycle 1

                                        if (lframe_nreg = '1') then
                                                LPC_State <= WSYNC;
                                        else
                                                LPC_State <= IDLE;
                                        end if;

                                    when WSYNC =>   -- Write Data Sync Cycle
-- Note: No device to respond with a synch at I\O addr
-- 080h. Therefore bus should time out and abort.
-- State ==> to IDLE
                                        if (lframe_nreg = '1') then
                                                LPC_State <= WPTAR;
                                        else
                                                LPC_State <= IDLE;
                                        end if;


when WPTAR =>    -- Write Data Final Turn Around Cycle
-- (not needed -- see WSYNC)
                                        LPC_State <= IDLE;          -- I/O write cycle end

                                    when others =>
                                        LPC_State <= IDLE;          -- all other cases
                                end case;
                        end if;
                end if;
end process;

P_sseg_decode: process(lclk)                                    -- decode section for 7 seg displays
begin
        if (lclk'event and lclk='1') then

                case W_Data(7 downto 4) is                      -- Most sig digit for display
                        when    "0000" => seven_seg_H <= "00000011";        -- Hex 03 displays a 0
                        when    "0001" => seven_seg_H <= "10011111";-- Hex 9f displays a 1
                        when    "0010" => seven_seg_H <= "00100101";        -- Hex 25 displays a 2
                        when    "0011" => seven_seg_H <= "00001101";        -- Hex 0d displays a 3
                        when    "0100" => seven_seg_H <= "10011001";        -- Hex 99 displays a 4
                        when    "0101" => seven_seg_H <= "01001001";        -- Hex 49 displays a 5
                        when    "0110" => seven_seg_H <= "01000001";        -- Hex 41 displays a 6
```

```
                when    "0111" => seven_seg_H <= "00011111"; -- Hex 1f displays a 7
                when    "1000" => seven_seg_H <= "00000001";        -- Hex 01 displays a 8
                when    "1001" => seven_seg_H <= "00001001";        -- Hex 09 displays a 9
                when    "1010" => seven_seg_H <= "00010001";        -- Hex 11 displays a A
                when    "1011" => seven_seg_H <= "11000001";        -- Hex c1 displays a b
                when    "1100" => seven_seg_H <= "01100011";        -- Hex 63 displays a C
                when    "1101" => seven_seg_H <= "10000101";        -- Hex 85 displays a d
                when    "1110" => seven_seg_H <= "01100001";        -- Hex 61 displays a E
                when    "1111" => seven_seg_H <= "01110001";-- Hex 71 displays a F
                when    others => seven_seg_H <= "00000001";        -- Hex 01 displays a 8

        end case;


case W_Data(3 downto 0) is                      -- Least sig digit for display
                when    "0000" => seven_seg_L <= "00000011";        -- Hex 03 displays a 0
                when    "0001" => seven_seg_L <= "10011111"; -- Hex 9f displays a 1
                when    "0010" => seven_seg_L <= "00100101";        -- Hex 25 displays a 2
                when    "0011" => seven_seg_L <= "00001101";-- Hex 0d displays a 3
                when    "0100" => seven_seg_L <= "10011001";        -- Hex 99 displays a 4
                when    "0101" => seven_seg_L <= "01001001";        -- Hex 49 displays a 5
                when    "0110" => seven_seg_L <= "01000001";        -- Hex 41 displays a 6
                when    "0111" => seven_seg_L <= "00011111"; -- Hex 1f displays a 7
                when    "1000" => seven_seg_L <= "00000001";        -- Hex 01 displays a 8
                when    "1001" => seven_seg_L <= "00001001";        -- Hex 09 displays a 9
                when    "1010" => seven_seg_L <= "00010001";        -- Hex 11 displays a A
                when    "1011" => seven_seg_L <= "11000001";-- Hex c1 displays a b
                when    "1100" => seven_seg_L <= "01100011";-- Hex 63 displays a C
                when    "1101" => seven_seg_L <= "10000101";        -- Hex 85 displays a d
                when    "1110" => seven_seg_L <= "01100001";-- Hex 61 displays a E
                when    "1111" => seven_seg_L <= "01110001"; -- Hex 71 displays a F
                when    others => seven_seg_L <= "00000001";-- Hex 01 displays a 8

        end case;
    end if;
end process;

end RTL;
```

Appendix B: List of Tables

Appendix C: List of Figures

Appendix D: Revision History

Table 62: Revision History

Revision	Date	Author	Changes
1.00 RC1.0	Jan 16, 2009	C. Eder	